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2000s

Exploring New Structure Devices

~ Integrated Circuit ~

One of the basic principles that has supported the development of the LSI industry to date is the MOSFET scaling law proposed by IBM's R. Dennard et al. In 1974. That is, by reducing the dimensions of a planar MOSFET fabricated on bulk Si at a physically constant ratio, it is possible to achieve higher integration and higher performance of the device. This proposal subsequently demonstrated its basic correctness as the miniaturization progressed, but on the other hand, it became clear that there were many restrictive factors such as the hot carrier effect, the deterioration of carrier mobility, the signal delay/reliability deterioration in Al wiring, tunneling current in the gate SiO_2 insulating film, etc. However, LSI engineers resolved these problems with new technologies such as LDD (Lightly-Doped Drain) structure, Cu wiring, strain channel, high-k/metal gate material adoption, and miniaturization continued uninterruptedly. However, as the design size became 100nm or less, the short channel effect appeared more severely, and suppression of leakage current and reduction of carrier mobility became severe, it became difficult to achieve both high speed and low power consumption. Furthermore, new factors such as statistical variation of channel impurities became obvious, and the necessity of a new MOSFET (CMOS) structure to replace the planar type by bulk Si came to be discussed.

The start of the new structure device was a partially depleted (PD) type device based on SOI (silicon-on-insulator). By fabricating a MOSFET on the SOI substrate, the parasitic capacitance of the drain was lowered, realizing high speed and low power consumption. Thereafter, various new structures such as planar type fully depleted (FD) SOI device, FinFET, multi-gate transistor, SiGe or Ge channel, and compound semiconductor channel were proposed. Of these, the FD-SOI device based on the planar structure has an advantage that the conventional planar technology can be used, but in order to suppress the short channel effect, thinning of the channel Si is severely demanded and the parasitic resistance thereof must be reduced. In a FinFET or a multi-gate transistor, even though it is not necessary to make the Si film as thin as a flat FD-SOI device, since the channel becomes three-dimensional, it is difficult to control its size. Further, in the case of Ge channel and compound semiconductor channel, consistency with Si technology, gate insulating film technology and the like become big problems. The figure shows the change of the MOSFET structure and the realization year, predicted by the ITRS 2009.

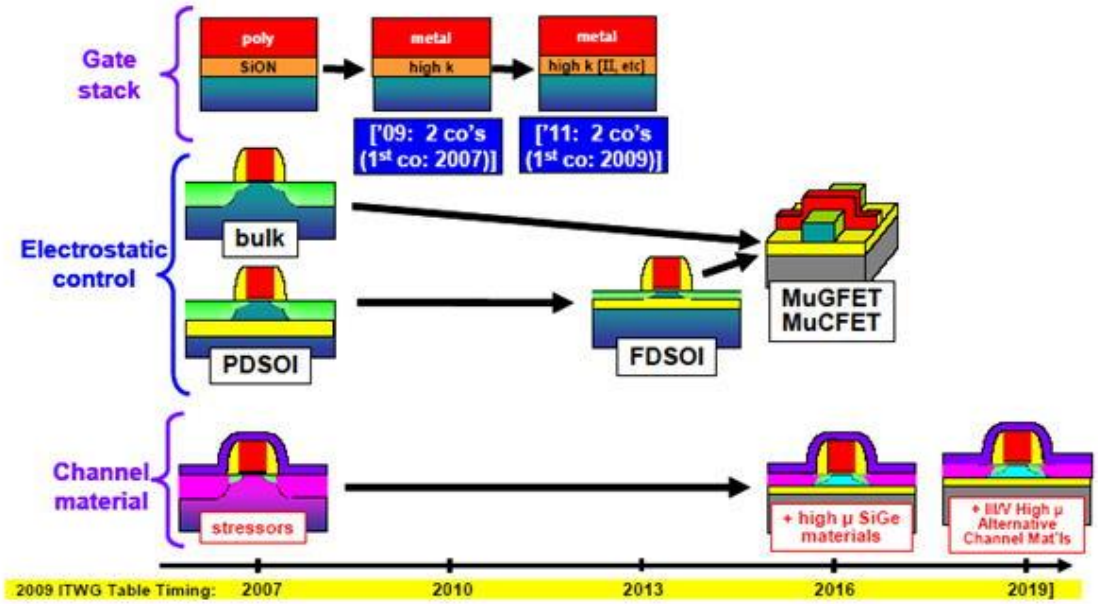

Figure: Prediction of structure change of MOSFET by ITRS 2009

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