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2000s

Enhanced interlinkage between design and production

~ Integrated Circuit ~

As the miniaturization of LSI advanced and the circuit became complicated, various variations in the manufacturing process of the LSI and the influence of defects due to particles and the like were increased, making it difficult to obtain LSI chips with good yield. Furthermore, the operation test of the LSI became more and more complicated, and its time and cost could not be ignored anymore. Meanwhile, as competition between device manufacturers intensified, early introduction of products to the market (time-to-market) by the shortening of development period (Turn-Around-Time) is required, and reduction of development/ manufacturing cost became a priority matter.
Therefore, DFM (Design for Manufacturability) attracted attention and came to be adopted, which attempted to obtain high manufacturing yield from the early stage of mass production even in state-of-the-art processes by the adoption of design methods which considered manufacturability from the circuit design steps. Furthermore, design for testability (DFT) such as Boundary Scan and BIST (Built in Self-Test) progressed in order to facilitate the operation test.

The concept of DFM had existed since the 1980s in lithography-aware layout design such as DRC (Design Rule Check). This was strongly recognized since the rapid progress of miniaturization from 130 nm to 90 nm and 65 nm, where the increase in parametric defects due to various manufacturing variations greatly affected the product yield. DFM first appeared in ITRS (International Technology Roadmap for Semiconductor) in 2005.
The specific contents of DFM varies widely, and the first approach began with attempts to correct the resolution in optical lithography with the OPC (Optical Proximity Correction) of the circuit layout pattern. Next, an analysis method of design margin was developed, that took into consideration variations in process and device characteristics due to operating environment fluctuations, and in parallel, the development was proceeded sharing the concept of DFM across the areas of design, process, EDA and manufacturing equipment. These developments included EDA (Electronic Design Automation) tools compliant with DFM, manufacturing equipment aware of circuit design, development of DFM verification method, etc.

On the other hand, the boundary scan is a technique for facilitating the test, and it is possible to use the test circuit embedded in the terminals of the LSI to perform the test of the board level terminals or the state of the terminals of the LSI without influencing the internal LSI operations. It was first proposed by JETAG (Joint European Test Action Group) in 1985. After that, as packages became increasingly dense by increasing the number of pins and by the adoption of BGA (Ball Grid Array), it came to be widely used as a test method for easily analyzing the connection state of the terminals, the voltage, or

the internal block circuit of the LSI.

By embedding the self-test circuit in the LSI, BIST not only can reduce testing cost by LSI testers, but also enables the test in the field after shipment. Furthermore, it enables the at-speed test of devices. The self-test is performed by generating a test pattern and comparing the output value with the expected value. BIST for memory has been used widely in SRAM since pattern generation is simple and expected output values are self-evident. In 1999, SynTest Technologies in the United States released a BIST design tool for SRAM. In case of BIST for Logic LSI, LFSR (Linear Feedback Shift Register) is connected to the scan chain, a random pattern is generated and applied, and the output is detected by MISR (Multiple Input Signature Register). Besides this, various BISTs such as BIST for analog/mixed signal LSI are in practical use. BIST is expected to continue to be developed as a core technology to facilitate LSI testing.

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