To search page

1980s

DRAM capacity increases, the shift to CMOS advances, and Japan dominates the market

~ Integrated Circuit ~

In the 1980s, Japanese manufacturers dominated the competition of DRAM memory capacity increase. The advance of Japanese manufacturers continued in 256 KDRAM following 64 KDRAM, and the global DRAM production share of Japan rose to 90%. However, this caused semiconductor commerce friction between Japan and the United States.

In the 256 KDRAM generation, the miniaturization progressed to the minimum line width of 2μm. The chip size increased, and it became difficult to maintain the yield at economical level. Therefore, a technique for improving yield was developed by adopting a defect repair method (redundant bit method) in which a defective memory cell was replaced with a spare memory cell. Japanese manufacturers began introducing the defect repair system from the generation of 256 KDRAM and it was generally adopted in 1 MDRAM generation.

One of the major changes in DRAM in the 1980s was CMOS implementation. In the NMOS scheme which had been used since the 4KDRAM generation, manufacturing process was simple, but it was becoming more difficult to maintain stable operation with low power in the shift to single 5-volt operation and higher access speed. The CMOS circuit system uses two types of transistors, PMOS and NMOS, and the process becomes complicated, but the circuit configuration is simplified. At that time the CMOS circuit scheme was already standard in logic ICs and SRAMs. In DRAM, too, the CMOS circuit method had many advantages in realizing functions such as low voltage operation and dual port memory dedicated to image processing. Toshiba and Hitachi began developing CMOS products of DRAM starting with 256 KDRAM generation.

At ISSCC in 1984 and 1985, CMOS 1MDRAMs were presented by Nippon Telegraph and Telephone Public Corporation, Hitachi, Toshiba, Mostek, and AT&T. Manufacturers which originally developed 1MDRAM with the NMOS circuit system switched to CMOS and CMOS DRAM was established as a standard. At the same time, the CMOS DRAM technology was developed as a high-speed and high-performance DRAM such as pseudo-static RAM (Pseudo SRAM), video RAM (VRAM), SCDRAM (static column RAM), high-speed page-mode DRAM, and it contributed to the expansion of application range of DRAM from main frame computers to rapidly increasing PC market. Intel, the pioneer of DRAM, withdrew from DRAM business at this time (1985), and it can be said it was a turning point in the industry.

At the same time, adoption of three-dimensional cells started. Reduction in storage capacity due to reduction in memory cell size by the advancement of miniaturization greatly reduced tolerance to soft errors, and the countermeasure was urgently needed. Although the effective film thickness of the capacitance film used for the memory cell had been reduced by using Si_3N_4 in place of SiO_2, it became insufficient in the continuing progress of miniaturization, and new schemes were proposed to increase

the storing capacitor area by three-dimensional cell structures. The proposals were "trench-cell method" in which holes (trenches) were made in a silicon substrate, whose side walls were used as memory cell capacitors, and "stacked-cell method" in which three-dimensional structures were formed on memory cells to increase the effective area of the memory cells. Each company developed 1 MDRAM prototypes by adopting these technologies. Both methods became mainstream of the memory cell system in the 4 MDRAM generation. Each of them had its merit and it was difficult to say one was better than the other. Different manufactures chose different schemes, and the capacity increase advanced after that with the coexistence of both schemes.

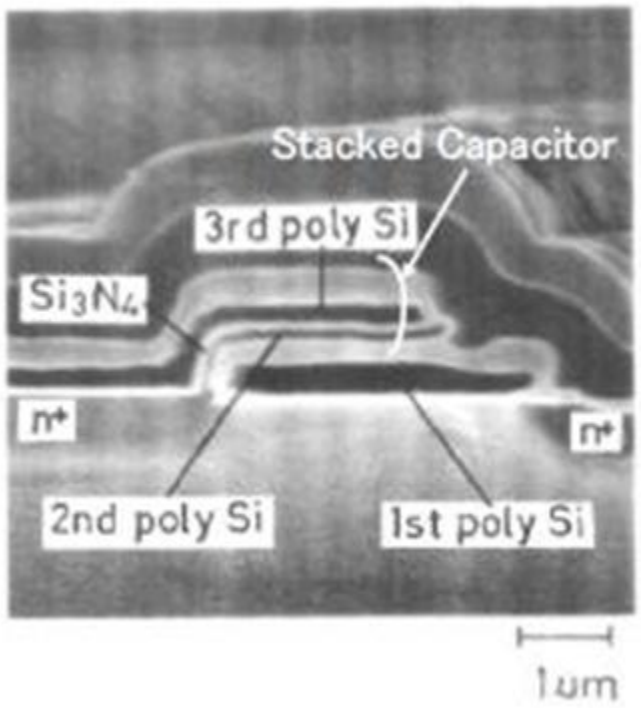

Fig. 1: Stacked Capacitor Cell, presented in 1978

Version 2019/1/23