To search page

Late 1990s

Adoption of the damascene method to form copper interconnect

Process Technology ~

From the beginning of LSI development, Al-based materials had always been used as interconnect materials, but as the miniaturization progressed, the electrical resistance of interconnects increased and signal delays on the signal lines and power loss on the power lines which were caused by the increase of RC (the product of interconnect resistance R and stray capacitance C) could not be neglected any longer in the LSI performance. Cu has a low resistivity of less than two-thirds of Al and is less expensive than silver and gold, so Cu had attracted attention from early on. Also, since the electromigration resistance, which is important in the interconnect reliability, is high with higher current density tolerance than Al by almost one order of magnitude, the shift from Al to Cu was a natural direction.

However, Cu was difficult to etch by RIE, hindering its practical use. With the advent of CMP, which was put into practical use since the late 1980's, the use of Cu interconnects in mass production advanced at a stroke in combination with damascene technology.

Damascene is a technique of inlaying, and as the word implies, grooves and holes are made in the portion of the insulation film where the interconnect is to be formed, and the metal (Cu in this case) is embedded in the groove. The metal which covers the part other than the groove is removed by CMP. RIE of Cu is not needed in the damascene process, and the surface is completely flat when the interconnects are completed. This makes it easy to form multilayer interconnects, and multilayer interconnects of 10 layers or more can be made.

Changes in interconnect materials and formation method also had a major impact on the equipment lineup. In the film formation, Al sputtering was changed to Cu sputtering and Cu plating, and Al RIE process was changed to oxide film RIE. Flattening process was changed from etch-back to CMP. In terms of sputtering technology, the in-plane uniformity was the main issue for the film formation on the flat surface in the case of RIE method interconnect, but in the damascene method, it is necessary to form a uniform film on the side wall of the deep hole or narrow and deep groove, and major technological innovations such as ionized sputtering have advanced. As equipment manufacturers, AMAT and Novellus System were famous, and as the domestic manufacturers, ULVAC and TEL followed.

Plating technology was adopted in the front-end manufacturing processes for the first time in the Cu damascene process. In order to fill the deep trenches, the bottom-up plating where the Cu film preferentially grows from the bottom of the groove to the top was necessary, and development of plating material solutions and equipment were advanced at a rapid pace. Initially, Novellus, AMAT, Semitool, Ebara, etc. competed, but now Novellus is mainstream.

It was IBM that led in damascene technology. It announced the successful prototyping of 0.25μm CMOS at the IEDM at the end of 1997. And it also made a press announcement of MPU product applying Cu multilayer interconnect, which greatly influenced semiconductor makers around the world. Since that time, transition to the Cu interconnect in various semiconductor companies was accelerated. Power PC in 1999 is famous as a product in which Cu interconnect was practically used. In Japan, commercialization of Cu damascene interconnect was promoted since 0.18μm CMOS generation, which was one generation behind IBM.

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