Towards User-Friendly Integrated Circuits

Dataquest Conference, Invited Speech, Hakone, 1986

Commentary

This conference, hosted by Dataquest, was held in Hakone, Japan. Although the speech was made in Japanese, materials were prepared in English.

The year of 1986 was the second year of the memory recession which started in the previous year, and all semiconductor manufacturers in the world were suffering. In 1985, Intel withdrew from the DRAM business, and SIA (Semiconductor Industry Association) of the US filed a lawsuit against Japanese memory manufacturers for dumping. The Japan-US Semiconductor Agreement was concluded in 1986 as the result of negotiation between Japanese and US Governments *(See note below).*

Industry participants were searching for a new direction towards more custom oriented business rather than standard, general purpose products such as memories and microprocessors. User-friendly IC (UFIC) was proposed as one of those concepts. The basic idea was to provide products to users which meet their needs in a short delivery time, and at reasonable price. Hitachi's ZTAT MCU was taken up as a representative example of such concept. ZTAT stands for Zero Turnaround Time which means TAT is essentially zero for users since the MCU programming can be done at their site using ZTAT MCU products in the inventory, which normally takes months in the case of conventional mask programming MCU.

The word "UFIC" was not established in the industry in the end. A major reason was that someone of overseas marketing group of Hitachi appealed the word sounds somehow strange to native speakers, and we stopped using it. The concept itself, however, helped formulate the cyclical nature of the semiconductor industry which was named Makimoto's Wave on the Electronics Weekly (UK) in 1991.

On the other hand, the word ZTAT was used as a byword for field programmability and became the forerunner of Flash-on-Chip MCU which is a mainstream of today.

This material was digitalized from paper based material, and there are some portions which are hard to read. I apologize for the inconvenience.

Note: Impact of US-Japan Semiconductor Agreement

Japanese semiconductor industry was badly affected by this agreement. Firstly, Japanese government strongly encouraged Japanese users to purchase foreign made products, and secondly, memory manufacturers lost freedom of price-setting which was provided by US government based on the cost data from each manufacturer. This Agreement is regarded as one of major reasons why Japan lost competitiveness in the semiconductor field in the global market. See Exhibit I, Episode 16 for more detail.

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TOWARD USER-FRIENDLY INTEGRATED CIRCUITS

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In April 1986 when the speech was given, it was soon after I took office as the General Manager of Musashi Works, the main plant of Hitachi semiconductor. In the situation of continuing memory recession from the previous year, we needed some strategic scenario to get out of it.
In this background, this presentation was aimed to discuss about technology and marketing strategy at the turning point of times. Here proposed was a new user-friendly IC (UFIC) concept, and its representative product was the ZTAT MCU.

1. Movement towards User-friendly Circuitry

Recent years have seen the appearance of a variety of words to describe semiconductor products aimed at specific user or application needs. One such expression is ASICs, short for application-specific integrated circuits, which was first coined by Dataquest, Inc. There are, however, several other terms in use, as can be seen from Fig. 1.

Looking at this list, there seem to be many differences of nuance from expression to expression; yet, there also seems to be a common thread tying them together. In each case, the designer, manufacturer, or whomever, seems to be aiming at what could be called user-friendly integrated circuits, or UFICs. Again, though, this UFICs term itself is not something that can be defined in great detail, but is rather only indicative of a broad current.

Over the past decade, the semiconductor industry has been predominantly geared toward producing high-performance and highly functional, yet standard, microprocessor and memory devices. The next ten years look to be a UFICs decade, however, with quite a few such devices already proposed or realized. Many more more-sophisticated UFICs are sure to appear in the very near future (see Fig. 2).

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Movement toward user-friendly IC

In recent years, we see many new words of products aiming for customer orientation (Fig. 1). ASIC, which is a newly coined word by Dataquest, is one of them. Such new words can be summarized in the word of User Friendly IC (UFIC) as a whole. In the past ten years MPU and memory occupied the mainstream of semiconductors, but the next decade will be the era of UFIC. Several UFICs have already appeared, but more will come out from now on. It is a group of products which meet customer needs, with improved cost performance and short TAT.

No matter what the UFIC. though. it will need to display high performance and sophisticated functions. Moreover. it will need to meet extremely specialized customer needs. And. it will need to do so in a way guaranteed to minimize necessary lead time to the greatest possible extent.

2. Why UFICs?

Tremendous improvements in user systems have been the result of the ongoing advances being made in semiconductor technologies. One major area of progress is in decreasing the number of required system componenents (Fig. 3). A particularly appropriate example is hand-held calculators. because of the important role they have played in driving early-stage MOS development.

Progress has been remarkable. Early on. these calculators made use of thousands of transistors and diodes. With advances in IC technology. the number of components was then reduced to 2-300. Moving on to the LSI era. it has finally became possible to configure the entire calculator circuitry from only a single chip. What is more. major improvements have also been registered in ease of function execution. power consumption and a variety of other areas during this same period. Current state-of-the-art is a calculator with virtually the same dimensions as a business card.

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Why UFICs?

Advances in semiconductor technology have created significant progress in electronic systems. Particularly great progress is reduction in the number of parts. The progress of calculators is a remarkable case (Fig. 3), in which the number of parts that once reached thousands of pieces has now become one chip LSI, and business card size calculator has been realized.

Advances in IC integration are also playing a major role in reducing the number of necessary components in many other types of systems and equipment (see Fig. 4). Looking at TVs, the early 1970s saw a one order drop from the need for hundreds of transistors and diodes to the need for tens of them. At the present, television sets are being manufactured with use only of a few ICs or LSIs and a few tens of transistors and diodes. Progress in the facsimile terminal area also is remarkable. Again, hundreds of ICs were required early in this decade. Now, however, sets are coming out that embody only a few tens of such integrated circuits.

The advances referred to in semiconductor technologies have come together with progress in other areas to facilitate development of so many sophisticated and convenient equipment systems that could not even have been envisioned only a few years ago. Whether in the form of personal computers or auto-focussing cameras, supercomputers or digital telecommunications switching equipment, industrial robots or what have you, examples are almost too numerous to name. Semiconductor technology progress has supported reduced costs and expanded applications in systems making use of ICs, thus in turn contributing to a huge expansion in demand for the very same semiconductor devices. This explosion of demand has itself provided the driving force for further technological leaps, thus working out very symmetrically.

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Due to advances in ICs, the number of parts of many electronic equipment has been reduced (Fig. 4). In the case of televisions and facsimiles, hundreds of parts dropped to dozens. Furthermore, due to advances in semiconductors, products that have never been imagined are on the market; personal computers, auto focus cameras, supercomputers, digital telephone exchangers, industrial robots and so on. Advances in semiconductors have brought about a reduction in the cost of electronic equipment which created great new demands. As a result, semiconductor technology has made further progress creating synergistic effects.

New types of semiconductor products are, however, becoming necessary as a result of these trends toward greater integration and expanded application areas (see Fig. 5). The application system designers and manufacturers making use of such devices are faced with developing and marketing systems that not only fit the needs of end-users to the greatest possible extent, but that also display some distinguishing difference from those systems put out by their competitors. When ICs were not so highly integrated it was possible to provide such distinguishing characteristics through unique arrangements of standard LSIs. In this time of VLSIs and ULSIs, however, such arrangements have to be made on the actual chips themselves. Applied system developers accordingly need chips that match the systems they are in the process of putting together.

Looked at from the semiconductor manufacturer side of things, there are other problems arising in this period of increasingly greater integration. Leaving aside the general-purpose megabi memories and high-end microprocessors now becoming possible for the first time, the combination on a single chip of 4/8 bit CPUs and peripheral ICs that used to be individual chips in themselves has thrown into danger the whole general-purpose nature of such LSIs. At this juncture, UFICs look to have a major role to play in dealing with the problems faced by both application system developers and semiconductor manufacturers.

Based on the discussion above (see Fig. 6), UFICs can possibly be defined as devices that will facilitate movement from a user's

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Due to the increase in integration density, both semiconductor users and manufacturers are facing major challenges (Fig. 5). Equipment makers must respond to the needs of end users and must differentiate themselves from competitors at the same time. Previously, this was made possible by a combination of small scale ICs, but from now on it is necessary to customize the chip itself.
For semiconductor manufacturers, small-scale devices have versatility, but versatility is lost with increasing integration level. UFIC is a device aiming at minimizing TAT from system concept to implementation, and it can be said that it is a desirable direction for both equipment makers and semiconductor manufacturers (Fig. 6).

system concept to implementation of the actual system in the shortest possible amount of time--that is. realization of the quickest possible turn around time.

Considering any system to fundamentally consist of both hard and software. two things look to be of increasingly greater importance in the software area: supply of sophisticated support tools that will speed-up software development by the user. and provision of field programmable LSIs that will facilitate the quickest possible writing into the device of the developed software. In the hardware area the key appears to be how to get the chips fitted to the needs of the particular user to him in the shortest possible amount of time. Here. design automation. or DA. has a vital role to play. This DA also needs to be capable of dealing with the problem of testability that is becoming increasingly more intractible as integration scale increases.

3. Underlying UFICs Technologies

3.1 Field-programmable Devices

There are two approaches to making the dedicated ICs that users now require (Fig. 7). First is by manufacturing mask-programmable devices. or MPDs for short. and the second via production of field-programmable devices. or FPDs. MPDs are customized during the wafer manufacturing process through use of.

Underlying UFIC's Technologies

There are two ways to create a specialized IC for users (Fig. 7).
One is a mask programmable device (MPD) and the other is a field programmable device (FPD).

hot masks designed to fit each particular device. Representative examples are mask ROMs and gate arrays. FPDs are LSIs where. after purchase from the manufacturer. the user can employ support-tool programmers to write-in software of his own specification. Examples here are electrically programmable ROMs. or EPROMs. and programmable logic devices. or PLDs.

With MPDs. it takes approximately one month or more before samples can be shipped to the user after an order has been received by the manufacturer. Because the user himself can undertake programming in a most simple manner with FPDs. however. turn-around time. or TAT. is reduced to virtually zero. Accordingly. FPDs can be labeled as being quite user-friendly.

Field-programmability would thus look to be a basic UFICs technology. Let's take a look. here. at an example.

Hitachi's ZTAT microprocessor is a plastic packaged microcomputer with a built-in EPROM. Compared to conventional single-chip microprocessors with internalized mask ROMs. this ZTAT facilitates a multitude of benefits. including:

1. ROM programming with a turn-around time of zero:
2. little risk of software bugs because there is no need for the user to order out his ROM programming: and
3. optimal suitability as a bridge to future mass production through use of later-developed masks (quick mass-production startup is possible and user opinions

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Typical examples of MPD are mask ROM and gate array, which take about a month from receipt of order to shipment. On the other hand, examples of FPD are EPROM and PLD, and users can program the devices by themselves. TAT is essentially zero and it can be said that it is very user-friendly.
Hitachi's ZTAT MCU is a plastic package version of MCU with on-chip EPROM, with following advantages: 1) TAT is essentially zero, 2) Negligible risks associated with bugs in ROM code, 3) Bridge to mass produced mask ROM products (finalizing the ROM code after completion of end-user's examination by the use of ZTAT products).

can be received and responded to before beginning mass production).

Development of this advanced type of device became possible upon consolidation of the several underlying technologies (refer also to Fig. 8):

1. high-performance microprocessor architecture;
2. CMOS EPROM techniques;
3. chip passivation to insure increased reliability, as well as plastic packaging techniques; and
4. highly efficient testing techniques for EPROMs and microcomputers accomodated together on the same chip.

Single-chip microprocessors with quick TATs were available before the advent of this ZTAT microcomputer (Fig. 9). However, comparing the ZTAT to conventional single-chip microprocessors with built-in mask ROMs should provide a clearer understanding of the advantages provided by this new device.

Microprocessors with internalized mask ROMS do provide economicality, yet the TAT needed for ROM programming is a problem. To achieve a quicker TAT, the piggy-back configuration made an appearance. What this entails is making it possible to place a commercial EPROM on the back of a microprocessor package. A virtually zero TAT could be achieved, but price problems appeared with this configuration. Microprocessors with built-in EPROMS accordingly next appeared on the scene. Because these were ultraviolet erasable PROMs, windows had to be equipped in

In order to realize ZTAT MCU, the following technologies were needed:
1) High-performance MCU architecture, 2) CMOS EPROM technology, 3) Passivation technology and plastic packaging technology to ensure reliability, and 4) Effective test method of EPROM embedded MCU.
Evolution to ZTAT is shown in Fig. 9. The mask ROM on-chip MCU is low cost, but with the problem of long TAT. A piggyback version carrying a commercially available EPROM on a package has a zero TAT, but the cost is very high. The EPROM on-chip version with UV-erase window also has a cost problem.

the packages. This made it impossible to drop prices down to suitable levels.

Finally, we come to development of the ZTAT. In appearance it looks the same as a conventional mask ROM, while the price is also close.

Let's look at what kind of applications have become possible as a result of development of this ZTAT (see Fig. 10). In the past there was little need to change the software to be written into a ROM. Moreover, mask ROM devices have been employed for applications where large numbers of chips are required. On the other hand, when the frequency of changes to software was high and the volume needed low, window-type microcomputers have been employed. In respect to intermediary applications, however, use of mask ROMs carries with it a risk, while use of window-type devices is expensive, thus facing the user with a dilemma.

ZTAT devices are ideal single-chip microprocessors for plugging this gap. The user can employ any number of chips whenever and wherever he desires. As you can see, then, UFICs aims have been advanced.

3.2 Electrically Erasable PROM (EEPROM) Technology

In comparison to EPROMs which are erasable with applied use of ultraviolet light, EEPROMs are PROMs which can be written and

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New application fields opened by ZTAT are shown in Fig. 10. So far, mask ROM versions have been used for mass-produced products with fixed ROM code, and MCUs with UV-erase window have been used for frequent rewriting and in small volume applications.
For medium-volume products, mask version has a risk of ROM code, and windowed version is expensive. It is the ZTAT version that fills this gap.

erased electrically. Though EEPROMs are larger than EPROMs, they offer major advantages in that a windowed package does not need to be employed and that programs can be written into them and changed even after the devices are assembled into a system. EEPROMs are accordingly a prime candidate for UFIC status.

EEPROMs have a long history (see Fig. 11). Only now, however, have 64 k-bit level devices come onto the market. Compared to the 16 k-bit circuits of only a few years ago, these now offer such advantages as:

1. a single, 5 V power supply rather than the previous dual source;
2. variable widths (byte-wide as well as chip-wide) for programming and erasure, greatly quickening these two activities;
3. high-speed operation; and
4. built-in circuitry that was formerly on peripheral devices.

The 64 k-bit devices are accordingly a lot easier to use.

Let's look a little more closely at these technological trends (Fig. 12). The cell area needed for one bit of EEPROM memory differs according to process resolution. At the same resolution, however, EEPROMs fall midway between DRAMs and SRAMs. In other words, while EEPROMs require two transistors per single bit of memory, DRAMs take one and SRAMs (in the Hitachi case) need four plus two resistors.

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Electrically Erasable PROM (EEPROM)

In the case of EEPROM, the ROM code can be rewritten even after it is incorporated in the system. This is a big difference from EPROM which requires ultraviolet ray for erasing, and it will become a leading player of UFIC. EEPROM has a long history (Fig. 11). At this moment, the 64K bit product has just become available. There are some advantages as compared with the 16K product, and much easier to use. The technology trend is shown in Fig. 12.

Taking Hitachi's EEPROMs as an example (see Fig. 13), cell size has tended to shrink to one fourth over a five year period. This has been accomplished not only by employing processes with finer line resolution but also by making use of a three-dimensional configuration (a tri-gate structure) for the two transistors needed for each bit.

There are two main technologies employed for EEPROMs: MNOS (or metal nitride oxide semiconductor), and floating gate (see Fig. 14). Each has its strengths and weaknesses; in short, MNOS provides a structure that is in principle simple, while the floating gate process is compatible with that for conventional EPROMs.

One current trend is to load an EEPROM on-chip. One such example can be seen in Fig. 15. This is an 8-bit microcomputer realized via a 2 um CMOS EEPROM process that provides, on-chip, 3 k-bytes of ROM, 128 bytes of RAM and a 2 k-byte EEPROM. A protection circuit is also provided which prevents external reading of written data without use of a stipulated procedure.

Sample applications (see Fig. 16) for just such a microprocessor with internalized EEPROM include:

1. individualized information registry taking the form of, for example, a credit or ID-type IC card;
2. precision machinery systems requiring fine adjustments: and

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In the case of Hitachi products, the memory cell size has been reduced to 1/4 in five years (Fig. 13). This has been accomplished, in addition to miniaturization, by the adoption of a three-dimensional tri-gate structure. The EEPROM structures include MNOS type and floating gate type.
The former has a simpler structure, and the latter is compatible with conventional EPROM process. Recently, there is a tendency to incorporate EEPROM on a chip, and an example of 8 bit MCU is shown in Fig. 15. Application examples of this MCU are shown in Fig. 16; writing individual information on IDs and IC cards,fine adjustment of precision machines, updating software of devices
located in remote areas, etc.

3. updating of software used in remote equipment.

Field programmability is, in this way, serving to meet the most minute user needs. Moreover, it is likely to be subjected to even further development in the future as a central UFICs technology.

3.3 Chip Design Automation

One fundamental UFICs feature involves getting the dedicated chip the user needs to him as fast as possible, as has already been mentioned (see Fig. 17). What this actually entails, however, is streamlining as well as fully automating the process from system to chip design.

In the days when integration density was not so great, it was possible for designers to manually put together circuits even when the logic was somewhat random or arbitrary. At the present day, however, where hundreds of thousands of transistors are being put onto one chip and the circuit diagram has become something several square meters in area, it is getting extremely difficult to do things manually. Disciplined design with DA backup is now becoming a vital requirement. What this "disciplined" design signifies is the modularization of logic, and structuring of the circuitry by means of a modular assembly approach. DA then involves automatic module design or automatic design of chips combining these logical modules.

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Chip Design Automation

The important point in UFIC is to deliver the ordered chip to the customer in the shortest time (Fig. 17).
In the era when the integration density was not high, manual design was good enough, but it is difficult to
manually deal with chips with hundreds of thousands of transistors today. Systematic design methodology by DA is indispensable on the premise of modularization of logic circuits.

The ultimate goal of DA is development of the necessary tools that make it possible to input the system concept and merely wait for the output of a silicon chip (see Fig. 18). Automatic design techniques are now being established for each stage from system to chip design. Accordingly, problems for solution in the near future are integration of each of these techniques in a total, overall process as well as automated realization of chips that compare favorably with manually designed chips in terms of chip size and performance.

With establishment of the optimal DA system as envisioned today (see Fig. 19), all the designer will need to do is describe system functions in a high-level language and confirm simulation results to realize a fully designed dedicated chip. The DA system will then undertake generation of a logical diagram from the input functions, generation of the necessary cells, layout of the overall chip through combination of these cells, and output of the data necessary for fabrication of the required hot mask. Simultaneously, a test pattern for confirmation of the suitability, etc. of the fabricated LSI will be automatically generated.

Currently, there are several ways to go about realizing dedicated LSIs (Fig. 20). These include a full-custom, standard cell, gate array, and PLD approach. In each case, the TAT and chip size characteristically differ. With the UFICs goal being minimum chip size with minimum turn-around time, it is apparent that a major DA system advance is now needed.

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The ultimate form of DA is that complete chip design automatically comes out if you enter the system description. If such a system can be created, what the designer does is to describe the system function in a high-level language and confirm the verification result. The DA system creates data for mask making based on this, and a test pattern for the LSI is generated.
Among several approaches for dedicated LSIs (Fig.20), the goal of UFIC is to realize the shortest TAT and minimum chip size.

3.4 Testability

Unfortunately, 100% of all manufactured semiconductors do not end up meeting original quality objectives (see Fig. 21). Accordingly, some kind of test is necessary for the culling out of defective products. One unfortunate result of the recent trend toward increasedly dense LSIs, however, is that chip testability has markedly decreased.

Just what signal strings will be output with input of just what signal strings--what is known as the test pattern is the series of signal strings that makes this determination possible. "Fault coverage" is a unit of measurement clarifying to what extent defects appearing in LSI circuitry can be detected. Comparing test pattern fault detection rates with the percentage of defective devices found among good quality devices at each sorting, it can be seen that the test pattern fault detection rate needs to be at least 90-95% for assurance of reasonable quality.

However, manpower required for realization of this 90-95% goal via use of fault simulators tends to increase greatly with LSI integration scale (see Fig. 22). This is because the number of places where defects may occur increase proporionately to the density of the circuit, and it accordingly becomes more difficult to monitor all such locations within the chip from "outside" the chip. Not only, then, is automatic design of the chip important.

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Testability

Since all products are not necessarily good products, some kind of test is needed. As the integration density increases, however, sufficient testing becomes more difficult. In order to ensure good quality, the fault detection coverage is required to be at least 90 to 95%. It is very difficult to manually achieve such a level (Fig. 22). Not only automation of design but also automatic generation of test patterns is required. One way to automatically generate test patterns is shown in Fig. 23.

but another vital requirement is automatic generation of the above-mentioned test patterns.

Let's take a look at one method of automatic test pattern generation (Fig. 23). With automatic addition of a test circuit covering all flipflops in any user logic circuit, it becomes possible to freely conduct flipflops and to read and write data from outside the LSI. Employment of this technique assures relatively simple automatic test pattern generation no matter how complex the chip.

5. Conclusions

"Systems on chip" have already begun to appear in calculator and watch applications. Semiconductor progress is sure to make it possible to realize other large-scale systems on a single chip. Depending on the application it will become necessary not only to integrate the CPU, memory and similar digital circuitry but also analog circuits on the same chip.

The UFICs that have been discussed in this paper are aimed at assuring that the user can freely combine a wide variety of semiconductor circuitry, with it ultimately becoming possible to mount it all on a single chip. Moreover, it must be possible to do this with minimum TAT, and within a minimum chip size. Once such devices make an appearance, it will become possible to offer truly friendly systems to end users, and to greatly improve the

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Conclusion

In the cases of calculators and watches, "system on chip" has already become a reality, and this trend
will spread. The goal of UFIC is to integrate all the circuit elements necessary for users on one chip, and to realize it with the minimum TAT and minimum chip size.

human/machine interface.

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TOWARD
USER-FRIENDLY INTEGRATED CIRCUITS

T. MAKIMOTO
MUSASHI WORKS
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ASIC : Application Specific IC
- Gate Array
  - Structured Array
- Standard Cell
  - Super Integration
- Programmable Logic Device (PLD)
  - Programmable Array Logic (PAL)

ASSP : Application Specific Standard Product
- Video RAM

ZTAT : Zero Turn Around Time

Fig. 1 UFICs RELATED TERMINOLOGY

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Fig. 1 New terminologies related to UFIC

ASIC and ASSP are coined by Dataquest, and ZTAT is the trade name of Hitachi.

SUPERIOR COST PERFORMANCE
SOPHISTICATED FUNCTIONS

+

SPECIALIZED CUSTOMER NEEDS
QUICK TAT

Fig. 2 UFICs REQUIREMENT

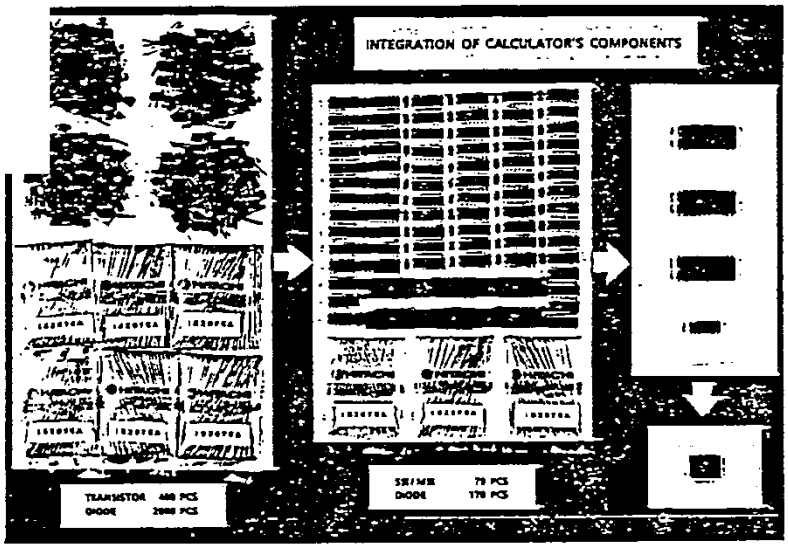

Fig. 3 INTEGRATION OF CALCULATOR'S COMPONENTS

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Fig. 2 Requirements for UFIC

Basic needs for UFIC are summarized here.

Fig. 3 Integration of calculator's components

Starting from thousands of transistors and diodes, one chip LSI has been realized through the advancement of semiconductor technology.

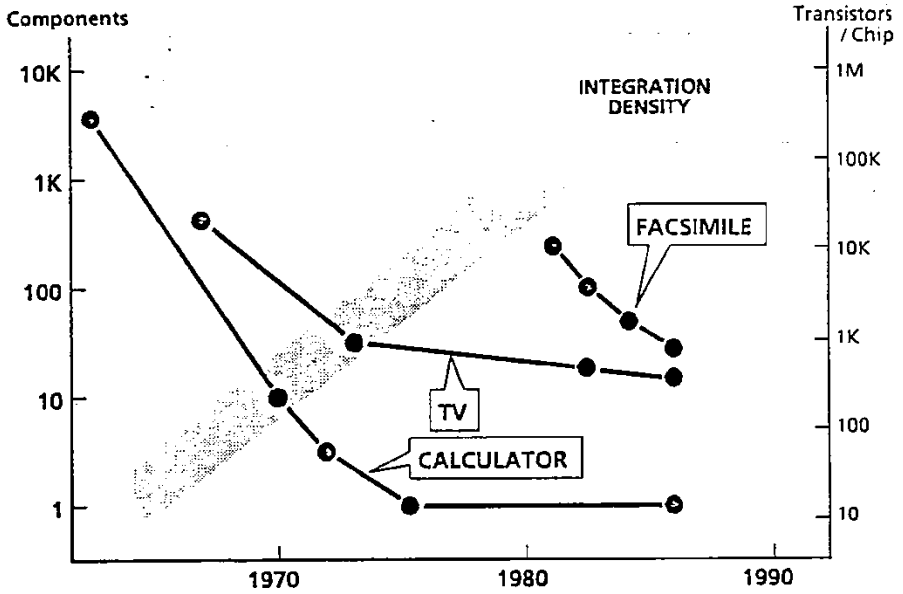

Fig. 4 DRASTIC DECREASE IN NO. OF COMPONENTS

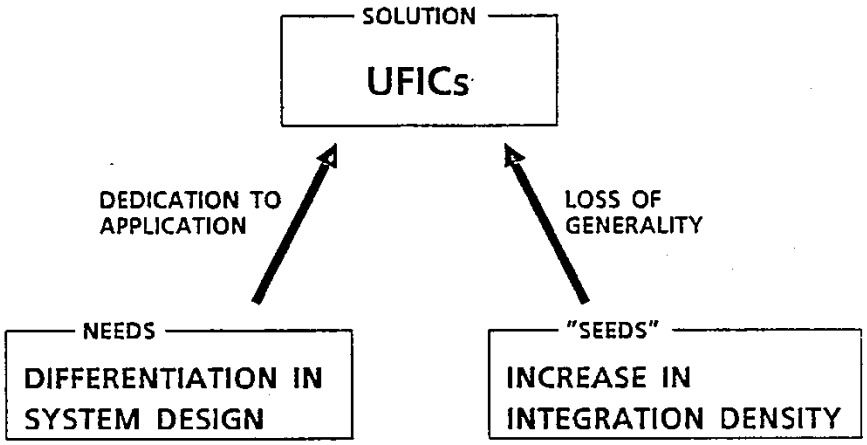

Fig. 5 WHY UFICs

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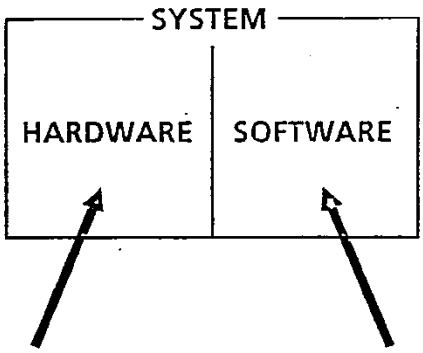
Fig. 4 Decrease in number of components

Number of components for calculators decreased from thousands to one. Number for TVs and facsimiles decreased to 1/10.

Fig. 5 Why UFICs?

Differentiation in system design is required from users, and increase in integration density is the technical seed to respond to the requirement. UFIC is the solution.



- DESIGN AUTOMATION FOR DEDICATED CHIPS
- TESTABILITY
- SUPPORT TOOLS FOR PROGRAMMING
- FIELD PROGRAMMING

Fig. 6 REQUIREMENTS FOR QUICK TAT FROM CONCEPT TO IMPLEMENTATION

— PLASTIC ENCAPSULATED EPROM ON-CHIP MICROPROCESSOR —

ZTAT OFFERS

- ZERO TURN AROUND TIME FOR MASK PROGRAMMING
- ZERO RISK OF ROM CODE ORDER PROBLEMS
- INTERIM SOLUTION BEFORE MASKED PRODUCT INTRODUCTION

Fig. 7 WHAT IS THE "ZTAT"

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Fig. 6 Requirements for quick TAT from concept to implementation

From hardware side, design automation and testability are important. From software side, support tool for programming and field programmability are needed.

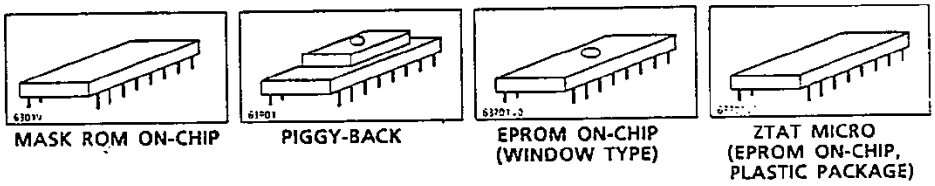
Fig. 7 What is ZTAT?

ZTAT is a plastic packaged EPROM on-chip MCU which offers zero TAT for programing, zero risk associated with ROM code ordering, and a role of bridge to the mask ROM version for volume production.

- HIGH PERFORMANCE MICROPROCESSOR ARCHITECTURE
- CMOS EPROM PROCESS TECHNOLOGY
- RELIABLE PASSIVATION AND PLASTIC PACKAGING
- EFFECTIVE TESTING OF MICROPROCESSOR / EPROM

Fig. 8 TECHNOLOGY UNDERPINNINGS OF ZTAT

— COST EFFECTIVE FIELD PROGRAMMABLE MICROPROCESSOR —



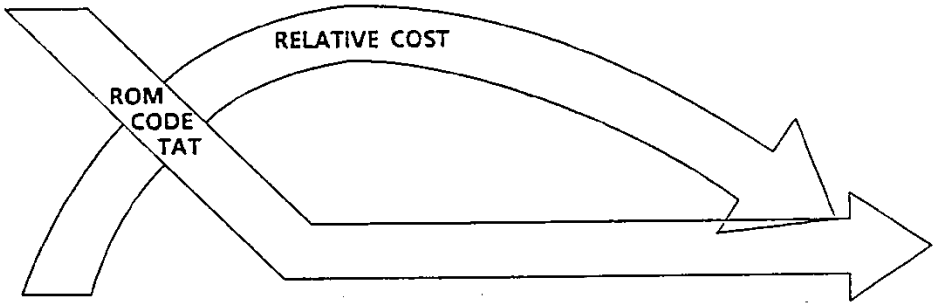


Fig. 9 ZTAT EVOLUTION

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Fig. 8 Technology base for ZTAT

Four new technologies were needed, as shown in the figure, to achieve the ZTAT product.

Fig. 9 Evolution to ZTAT

Relative cost and TAT are shown graphically for four types of MCUs, namely, mask ROM on-chip type, piggy-back type, EPROM on-chip type with window, and ZTAT type. The goal of ZTAT is to achieve cost level close to mask ROM type with zero TAT.

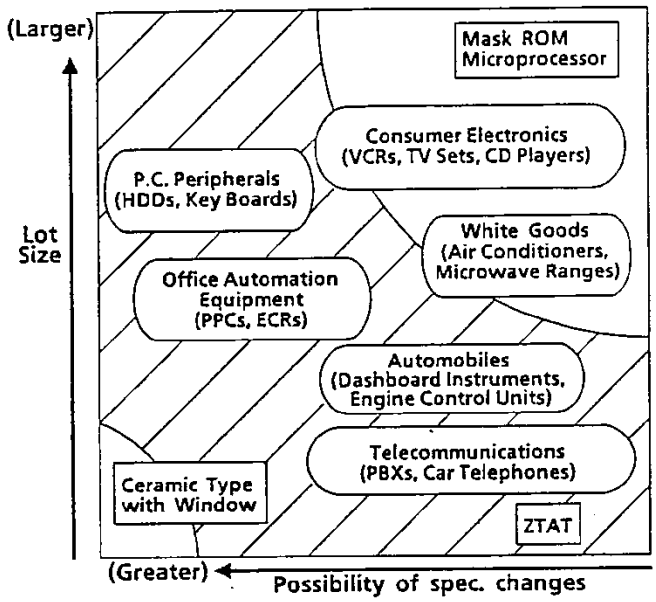

Fig. 10 ZTAT APPLICATION

1979	1985
K bit (2K×8)	64K bit (8K×8)
m N-MOS	2μm C-MOS
Double Power Supply	Single 5V
Chip Erase	Chip / Byte / Page Erase
Byte Write	Byte / Page Write
Read Access Time 350 / 450 ns	200 / 250 ns
Write Time 20 ms	10 ms
	Peripheral Circuits on Chip Address, Data Latches, Data Protection etc.

Fig. 11 EVOLUTION OF EEPROM TECHNOLOGY

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Fig. 10 Application fields for ZTAT MCU

Mask ROM version is for high volume application where ROM code changes happen rarely. EPROM version, either window type or piggy-back type, is for low volume application where ROM code changes frequently happen. ZTAT covers the intermediate fields such as PC peripherals, office automation, automobiles, and communications.

Fig. 11 Evolution of EEPROM technology

Comparison is made between 16K bit (1979) and 64K bit (1985) EEPROM devices based on 3micron and 2micron technologies respectively. Besides increase in the memory density, new functions are introduced for more ease of use.

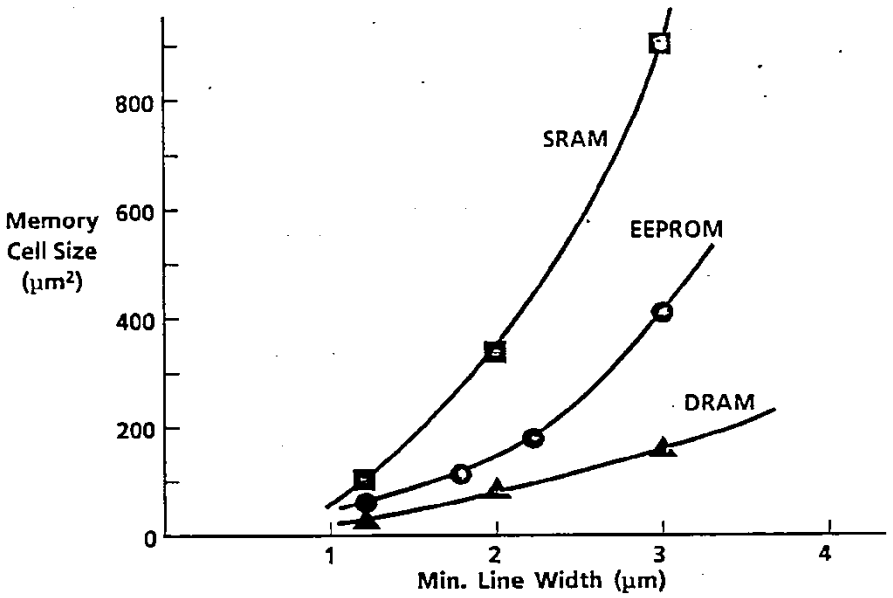

Fig. 12 CELL SIZE FOR MOS MEMORIES

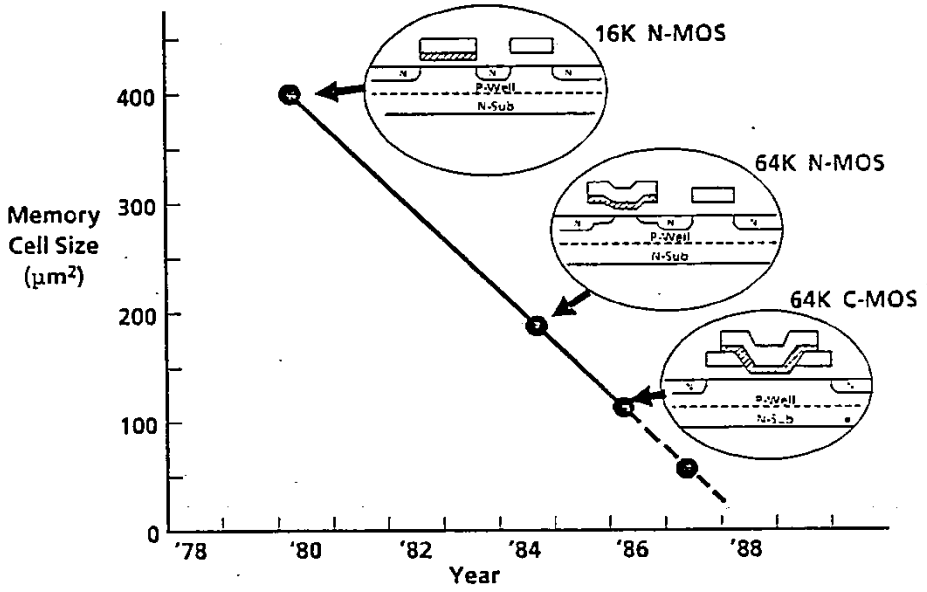

Fig. 13 EEPROM MEMORY CELL SIZE TREND

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Fig. 12 Cell size for MOS memories

The trend of cell size for DRAM, SRAM, and EEPROM is shown as a function of design rule. EEPROM is in the middle between DRAM and SRAM.

Fig. 13 EEPROM cell size trend

Trend of cell size for 16K bit (NMOS), 64K bit (NMOS), and 64K bit (CMOS) EEROM is shown. CMOS version of 64K bit device will be further shrunk compared to the NMOS version.

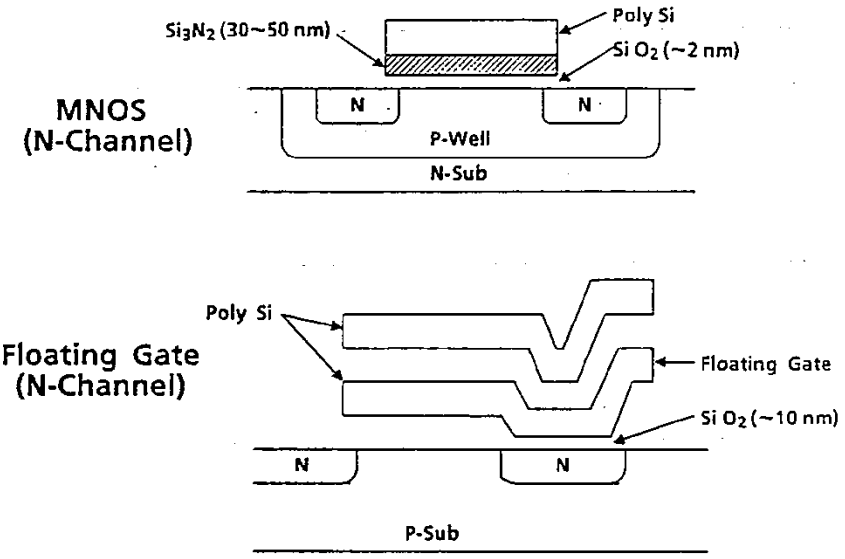

Fig. 14 EEPROM STRUCTURES

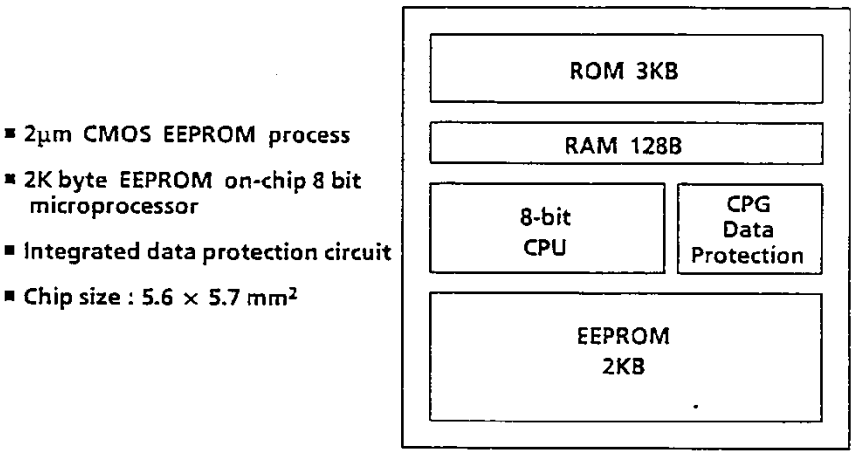

Fig. 15 EEPROM ON CHIP MICROPROCESSOR

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Fig.14 Cross-sectional structure of EEPROM cell

Cross sections of floating gate type cell and MNOS type cell are shown. MNOS is simpler in structure, and floating gate type is compatible with conventional EPROM structure.

Fig.15 EEPROM on-chip MCU

8-bit MCU equipped with 2 Kbyte EEPROM based on 2 μ CMOS process is shown. Data protection circuit is built in. This is a case of the state-of-the-art MCU at the time.

Type of Applications	Examples
Personal Information Storage	▪ IC Card (Bank Card, Credit Card etc.) ▪ Security System ▪ ID Card
Data Calibration	▪ TV Tuner Control ▪ Automotive Applications ▪ Robotics, Precision Control
In-Circuit Software Up-date	▪ Remote Controller ▪ Factory Automation

Fig. 16 APPLICATIONS OF EEPROM ON CHIP MICROPROCESSOR

- OVERALL AUTOMATION FROM CONCEPT TO SILICON CHIP

PROBLEMS TO BE SOLVED

- SYSTEM INTEGRATION
- CHIP COMPETIVENESS
  - CHIP SIZE
  - PERFORMANCE

Fig. 17 DESIGN AUTOMATION OBJECTIVES

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Fig.16 Applications of EEPROM on-chip MCU
Personal information storage (bank card, credit card, security system, ID card), data calibration (automobile, robot, precision control equipment), and software update (remote control, FA).

Fig.17 Objectives of DA
To consistently automate from concept to Si chip. Problems to be solved are system level integration and competitiveness of chip (chip size and performance)

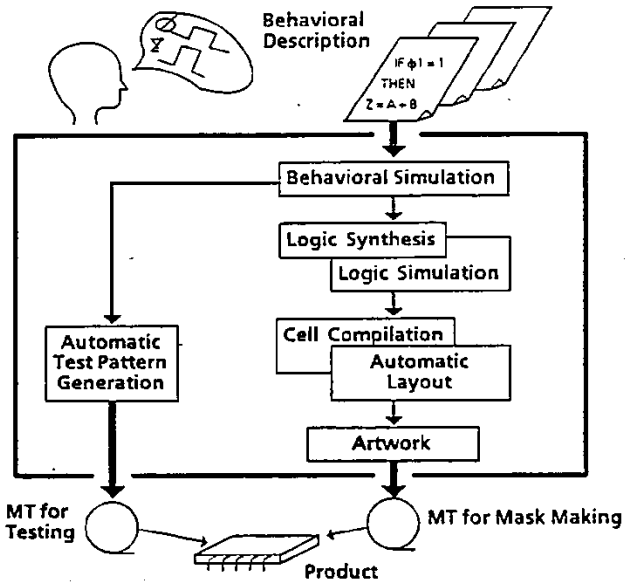

Fig. 18 INTEGRATED DESIGN AUTOMATION SYSTEM

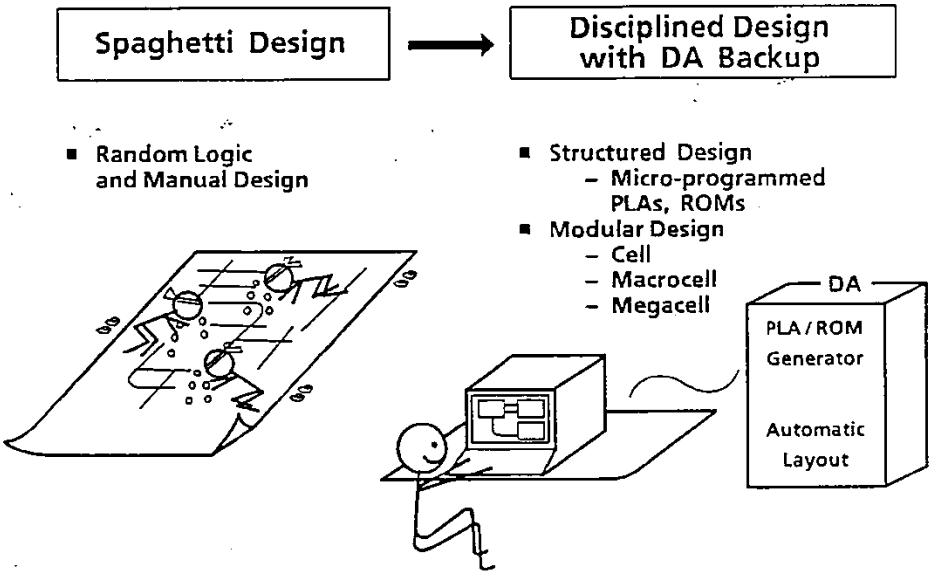

Fig. 19 DESIGN METHODOLOGY

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Fig.18 Integrated DA system

After the behavioral simulation, logic synthesis and layout design are performed, and mask data is automatically created. The test pattern is also generated simultaneously.

Fig.19 Design methodology

Traditional design methodology was “spaghetti design” done manually. From now on, a systematic design methodology based on DA is the must. It is also important to utilize large-scale cells such as macro-cells and mega-cells.

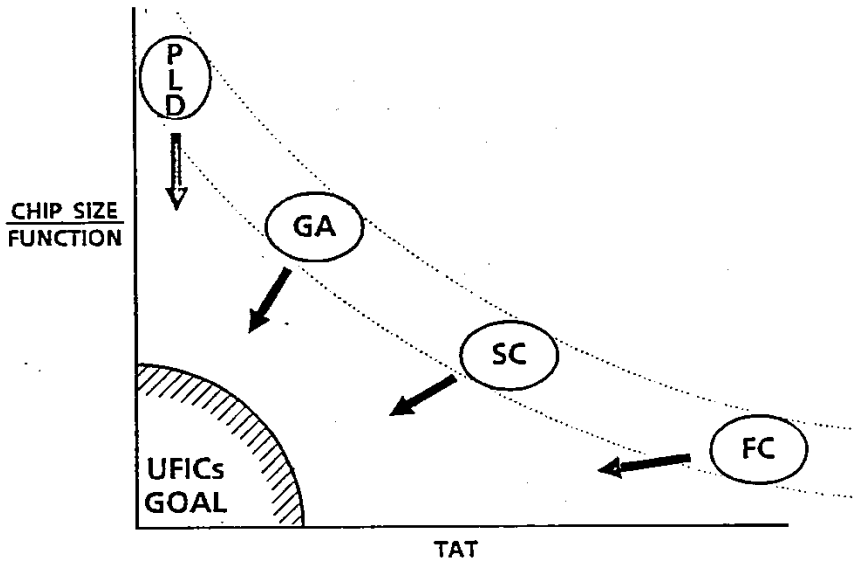

Fig. 20 TRADE-OFF BETWEEN TAT AND CHIP SIZE

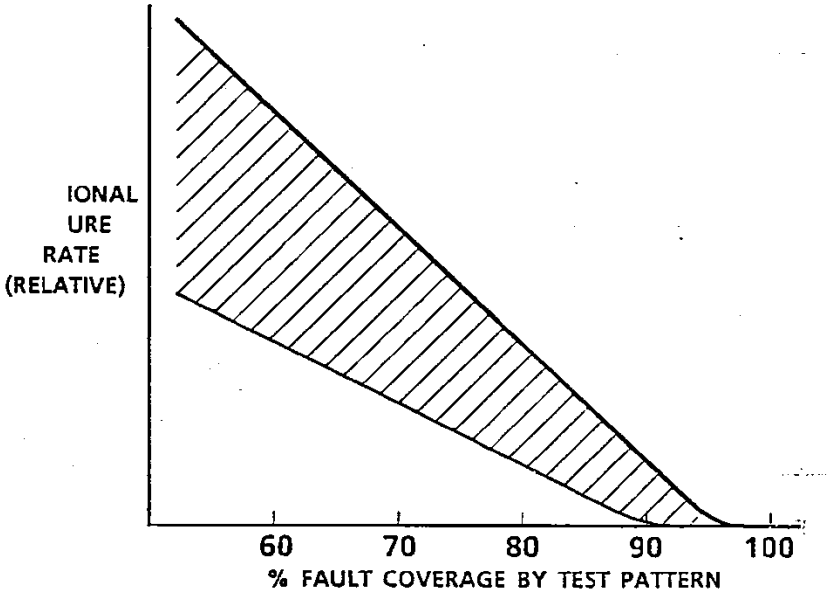

Fig. 21 PROBLEMS CAUSED BY POOR TESTABILITY

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Fig. 20 Trade-off between TAT and chip size

The figure shows the trade-off between TAT and chip size for PLD, gate array (GA), semi-custom (SC), and full custom (FC). The goal of UFIC is to achieve minimum chip size and shortest TAT.

Fig. 21 Problems caused by poor testability

If the fault detection coverage by the test pattern is low, the functional failure rate increases.

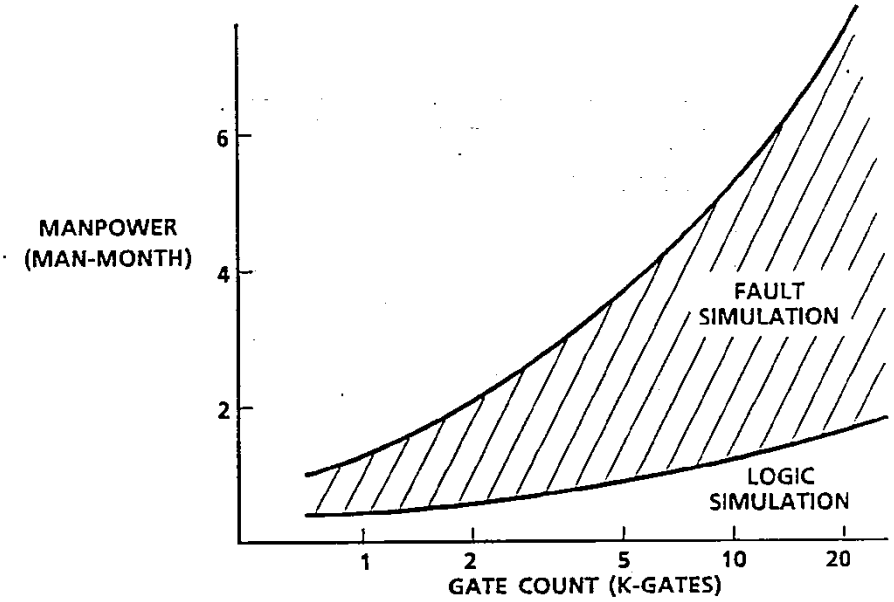

Fig. 22 MANPOWER REQUIRED FOR TEST PATTERN GENERATION

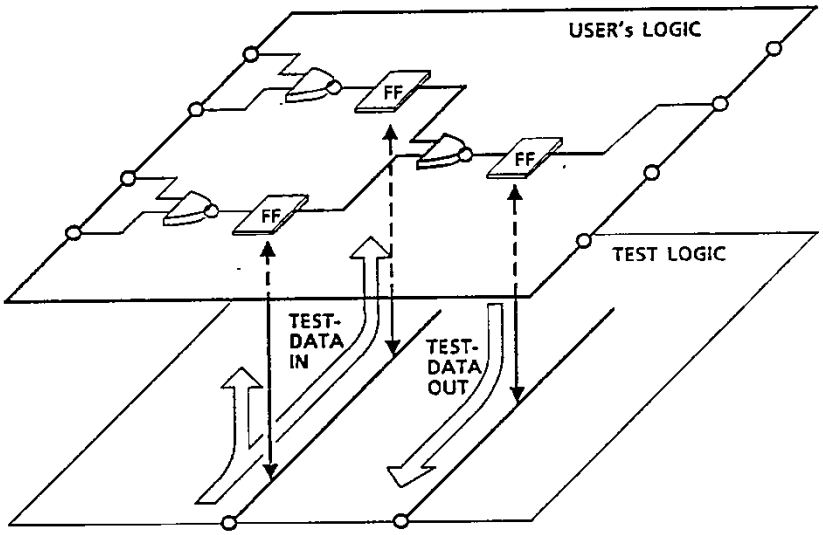

Fig. 23 AUTOMATIC TEST LOGIC ADDITION AND TEST PATTERN GENERATION

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Fig. 22 Manpower required for test pattern generation

As the number of integration density increases, the manpower for both logic simulation and defect simulation increases, but the latter increases more sharply.

Fig. 23 Automatic test logic addition and test pattern generation

This is a method of automatically inserting test circuits for input and output data to all the flip-flops in the logic diagram. The fault detection coverage is remarkably improved.

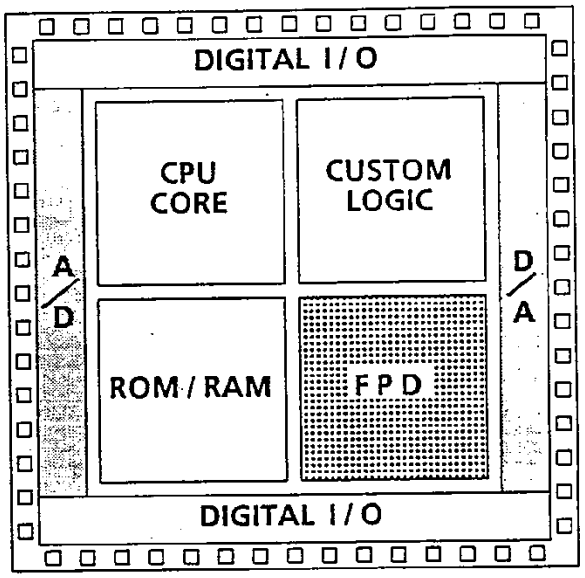

Fig. 24 FUTURE UFIC IMAGE

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Fig. 24 Future image of UFIC

In the future, UFIC will include CPU, memory, and custom logic with FPD (Field Programmable Device), and the functional flexibility will be considerably increased.
As is written in the "commentary" column, the word UFIC has naturally disappeared, but the concept
of Fig. 24 is very similar to the configuration of today's PSoC (Programmable SoC).