Evolution of Low Power Electronics and Its Future Applications

ISPLED, August 25, 2003, Seoul
Keynote Speech

Commentary

ISPLED is an abbreviation for "International Symposium on Low Power Electronics and Design". It is a conference where engineers and researchers gather in a wide range of technical fields such as process, circuit, system, architecture, and application for achieving low power VLSI. As the 8th conference this time, ISPLED which began in 1996 was held in Seoul in the Asian region for the first time. All previous meetings were held in the US.

One of Japan's global contributions in the field of low-power electronics was to push CMOS to the mainstream of VLSI in place of NMOS. It was from the late 1970s to the 1980s. On the architectural aspect, "low-power, high-performance" MPU was realized by the re-engineering of the RISC architecture, which opened up a new field of digital consumer segment.

In this speech, these points were outlined and introduced with some concrete examples. In addition, in the United States, the optimization of algorithms is progressing toward further lowering the power of the system, and some examples of achievements were introduced.

As a future application field, robots are becoming increasingly important, and it is predicted that they will become technology drivers for the semiconductors. In the future, the need for VLSI with "high performance and low power" will increase more and more.

ISLPED, Seoul
August 25, 2003

Evolution of Low Power Electronics and Its Future Applications

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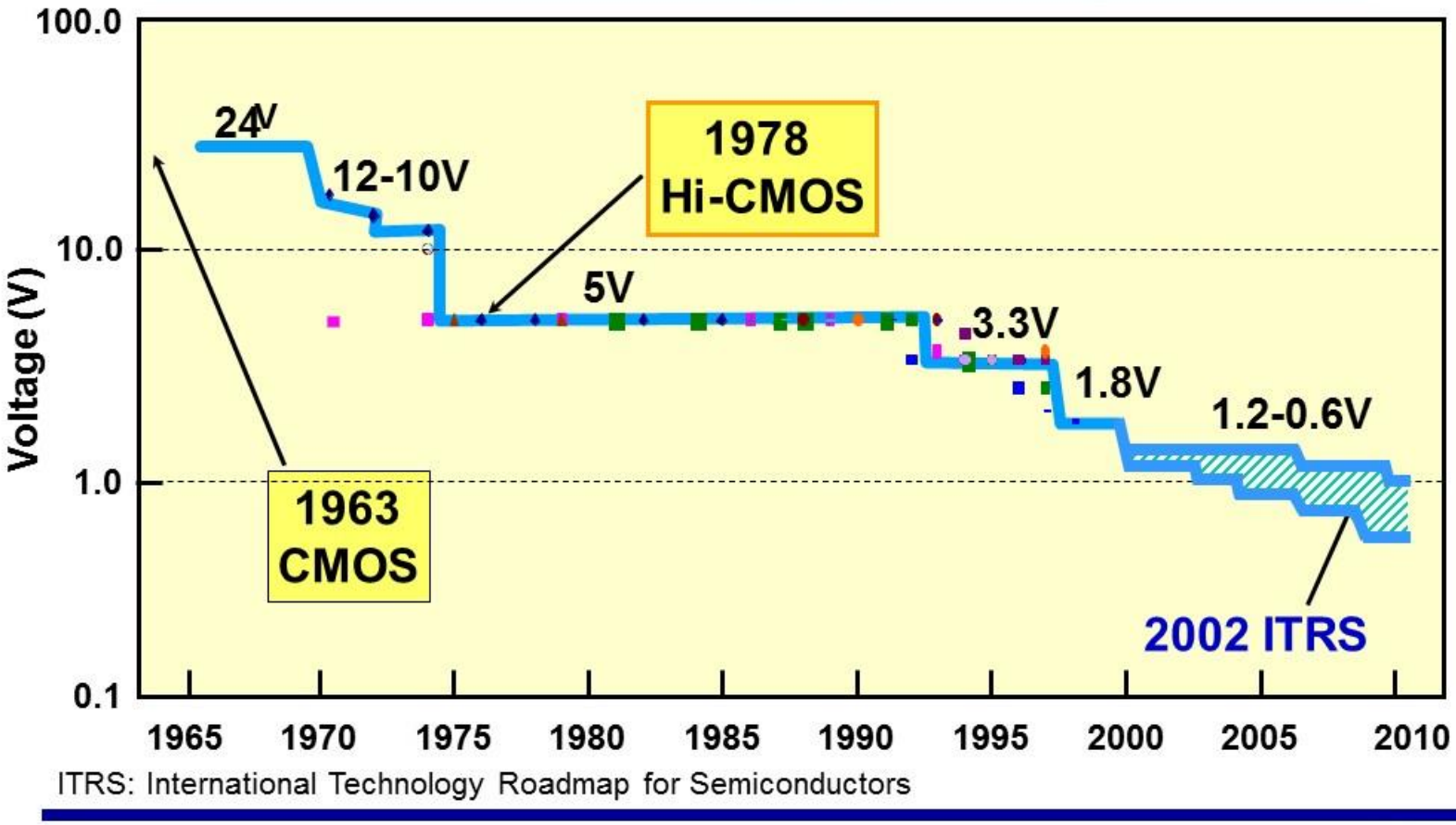
At this time, the need for "low-power and high-performance" LSI was increasing in digital consumer products including mobile phones. This speech describes the history of progress of low power technology of semiconductors and future applications.

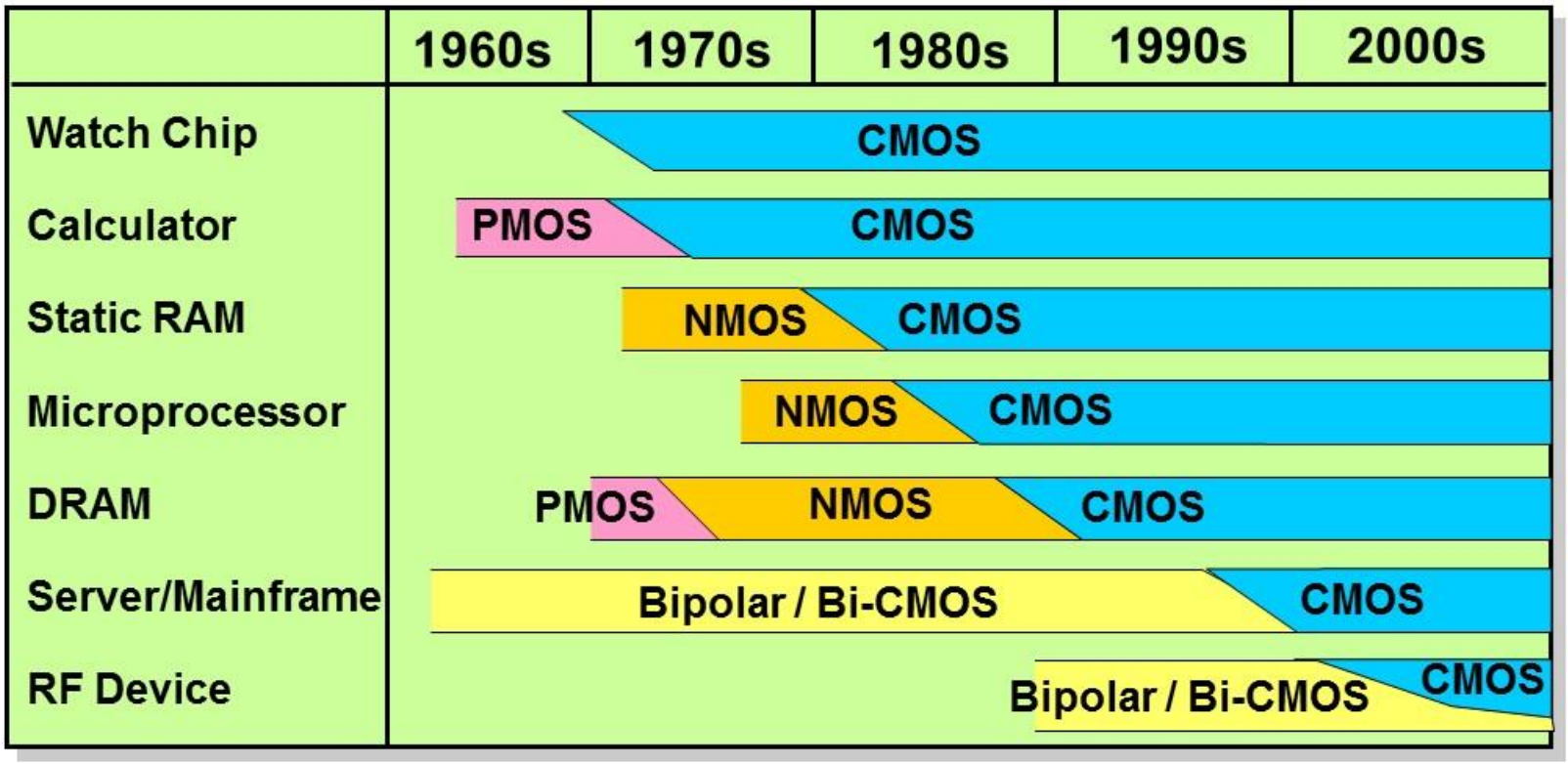
Outline

- Introduction
- Historical Review
- Architectural Innovation
- SoC and Emerging Markets
- Robots: The New Technology Driver



In order to realize low power, it is most important to lower the power supply voltage. It was 24V in the 1960s, and then reduced to 5 V in the 1970s, and it was the standard power supply voltage until the beginning of the 1990s. After that it was gradually lowered further, and it was shifting from 1.8 V to 1.2 V at the time of this speech. ITRS(2002) predicted that it will further decrease to 0.6 V in the future.

History of CMOS Convergence



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The figure shows how CMOS has spread as the deciding factor of low power technology. Initially it was limited to low speed / low power fields such as watches and calculators. The successful implementation of high-speed CMOS SRAM at the end of the 1970s changed the situation. In the 1990s it was used for mainframes, and today it is used for most IT equipment from small to large.

NMOS vs. CMOS for SRAM

	2147 / Intel (1977)	6147 / Hitachi (1978)
Product	HMOS 4K Static RAM	HiCMOS 4K Static RAM
Technology	NMOS	Twin-Well CMOS
Speed	55 / 70 ns	55 / 70 ns
$I_{Active}/I_{Standby}$	110 mA / 15 mA	15 mA / 0.001 mA
Chip Size	16.2 mm^2	11.5 mm^2

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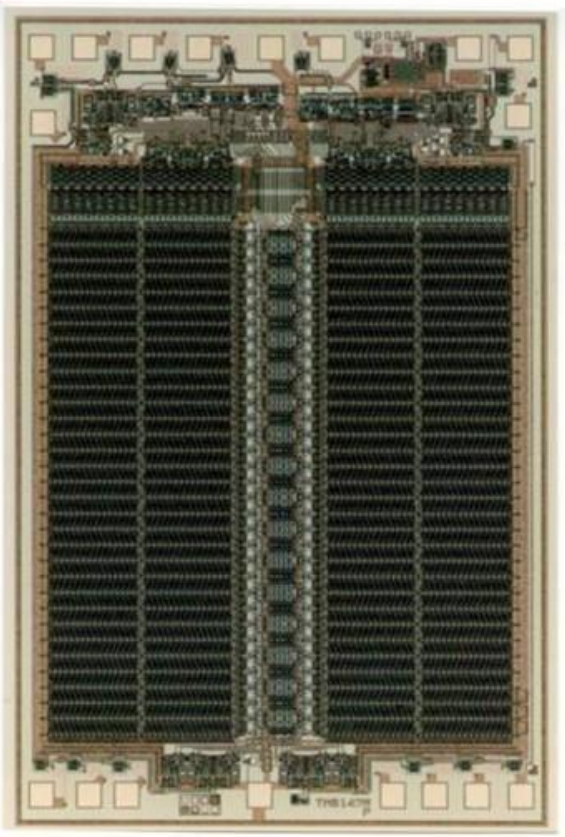
This table is a historic data showing the superiority of CMOS as the high speed device. In the late 1970s, Intel's 4K SRAM using NMOS technology boasted the world's fastest speed. In Hitachi, twin-well CMOS technology was developed, and achieved the same speed while taking advantage of low power characteristics. This data clearly showed that CMOS is the future direction of semiconductors.

HM6147: 4K Static RAM (Hitachi)

Source: Hitachi Ltd.



Chip Size:2.7mm x 3.95mm

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Hitachi's 4K bit SRAM which showed CMOS to be the future direction of technology was awarded the IR 100 Award of 1979, which was given to 100 outstanding new products each year (currently, R&D 100 Award). The award was the endorsement that the CMOS device was a breakthrough product. The chip photo is shown on the right.

NMOS vs CMOS for Microprocessors

		6801 / Hitachi (1979)	6301 / Hitachi (1981)
Product		8bit MPU	8bit MPU
Technology		4 Micron NMOS	3 Micron CMOS
Speed		1 MHz	1 MHz, 1.5MHz, 2MHz
Power	Active	900 mW	30 mW (f = 1MHz)
	Standby	70 mW	0.01 mW
Pin Count		40 Pins	40 Pins

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This table compares the performance of NMOS and CMOS version of 8-bit MPUs. They are compatible products with the same functions. The speed of the CMOS version is equal to or higher than that of the NMOS version, and the power is orders of magnitude smaller. The advantage of CMOS was proved also for logic products, and this accelerated the conversion to CMOS.

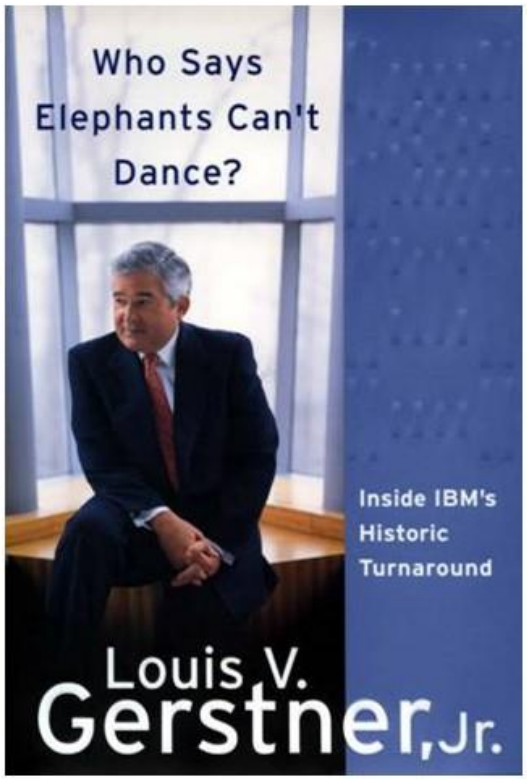
Change in Mainframe Architecture

- IBM's sales of mainframe was declining because of a precipitous drop in market share.

-The technical team made a bold move to a totally different architecture: from bipolar to CMOS.

- Had we not made the decision to go with CMOS, we'd have been out of the mainframe business by 1997.

Source:HarperBusiness, 2002



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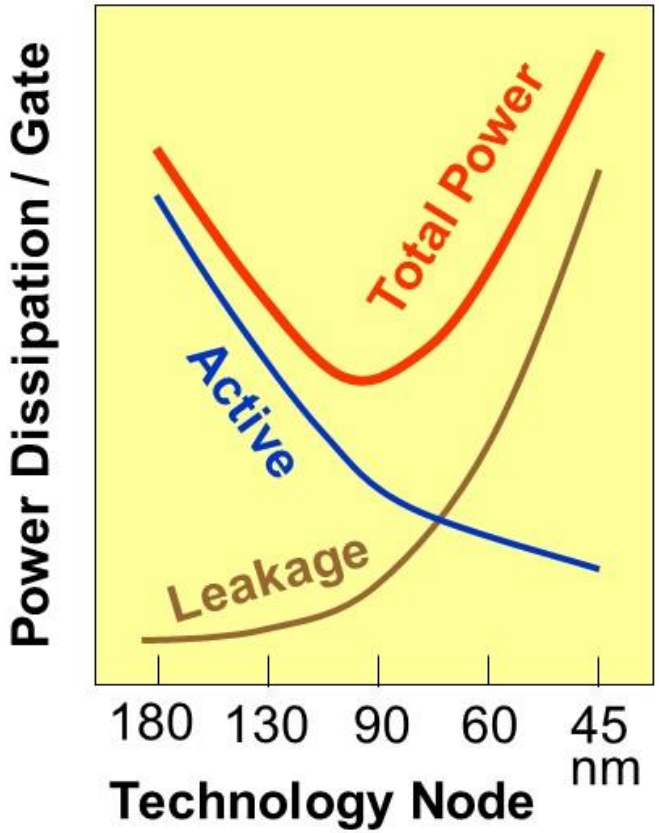
In the previous year of this speech, IBM's former CEO Gerstner published an autobiography "Who Says Elephants Can't Dance?". In the book, he recalls that IBM's mainframe business was saved by the decision to switch to CMOS. It is not usual for top executives of a computer company to touch on the device issue, and it can be inferred how important the decision of CMOS conversion was for IBM.

Future Challenges

- **Process/ Device**
  - ★High K Gate Material
  - ★Multi Threshold Voltages
- **Circuit/ System**
  - ★Gated Clock
  - ★Partial Power Off
  - ★Total Power Management
- **Strong Teamwork of Multidisciplinary Engineers**



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This shows challenges for the future of low power technology. The figure on the right shows that while the active power decreases with miniaturization, the static power increases by the increase of leakage current. How to minimize the total power is a big challenge. Strong teamwork of multidisciplinary engineers from process, device, circuit, and system, is required for getting optimum solution.

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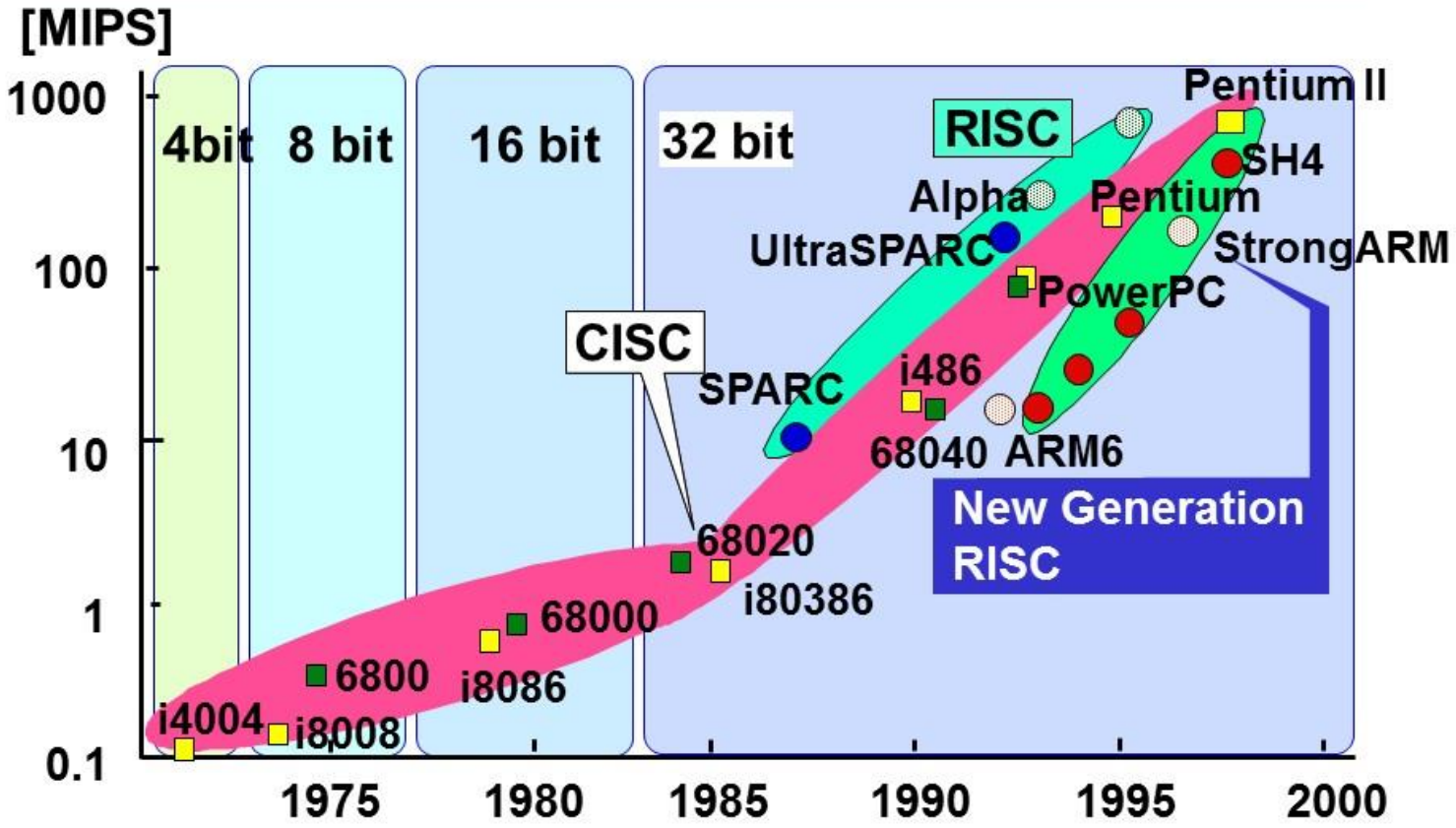
- **Architectural Innovation**
- SoC and Emerging Markets
- Robots: The New Technology Driver

Progress of Processor Architectures



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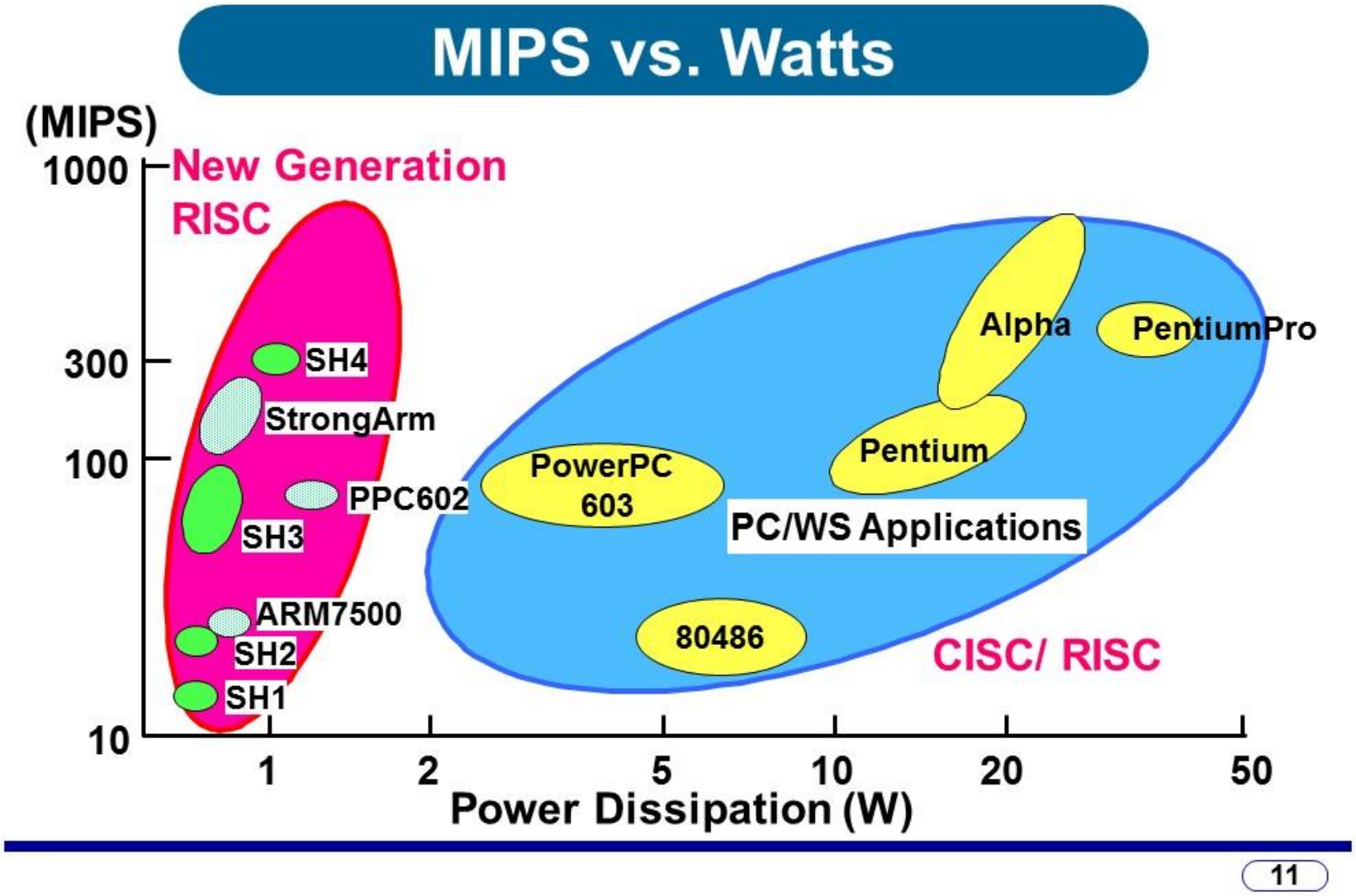
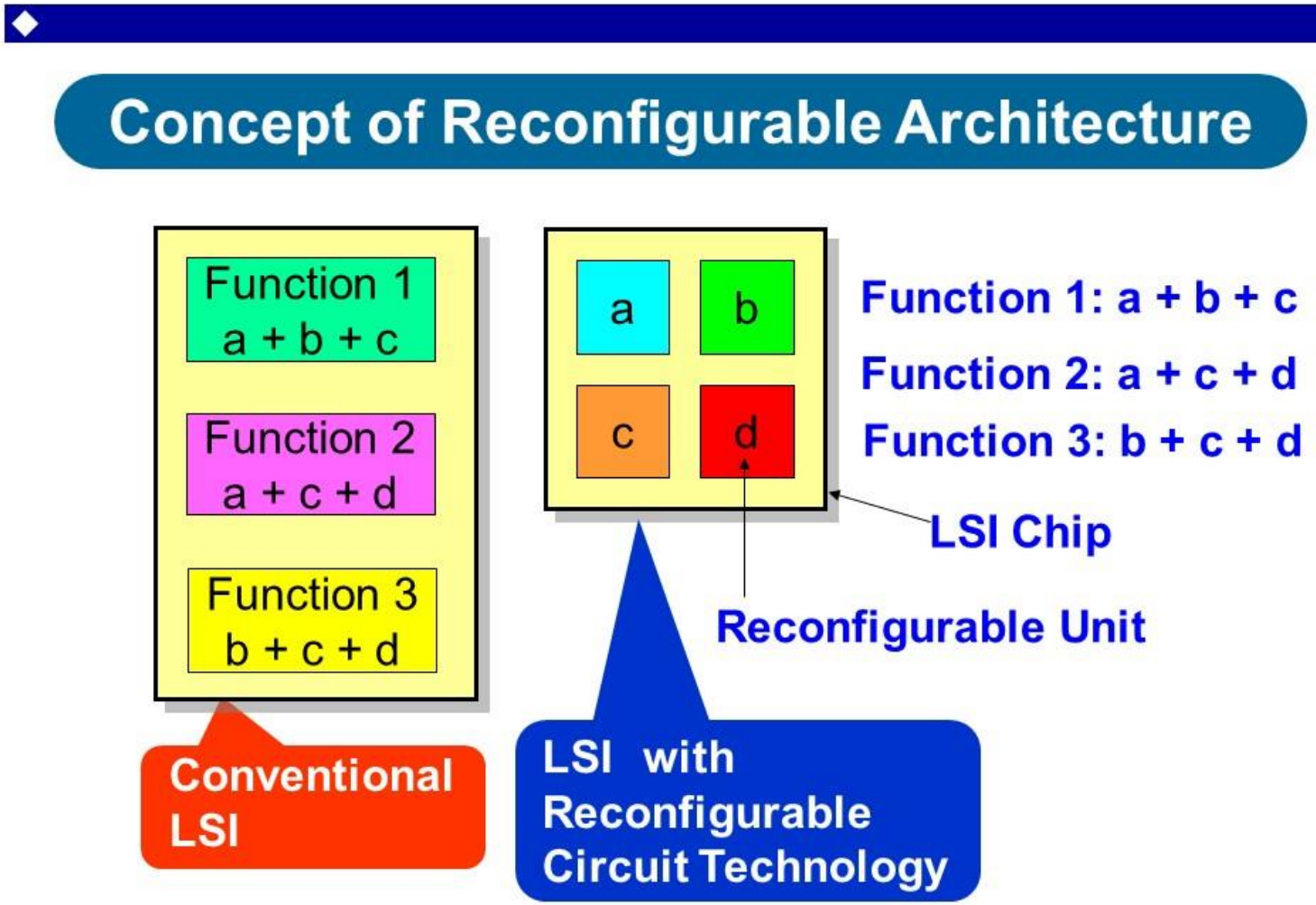
The figure shows the history of MPU architecture evolution. In the late 1980s RISC type was introduced and used for high performance equipment. By re-engineering the RISC in the mid 1990s, "low power and high performance" MPUs such as ARM and SH were commercialized as “new generation RISC”, and new application fields were developed one after another.

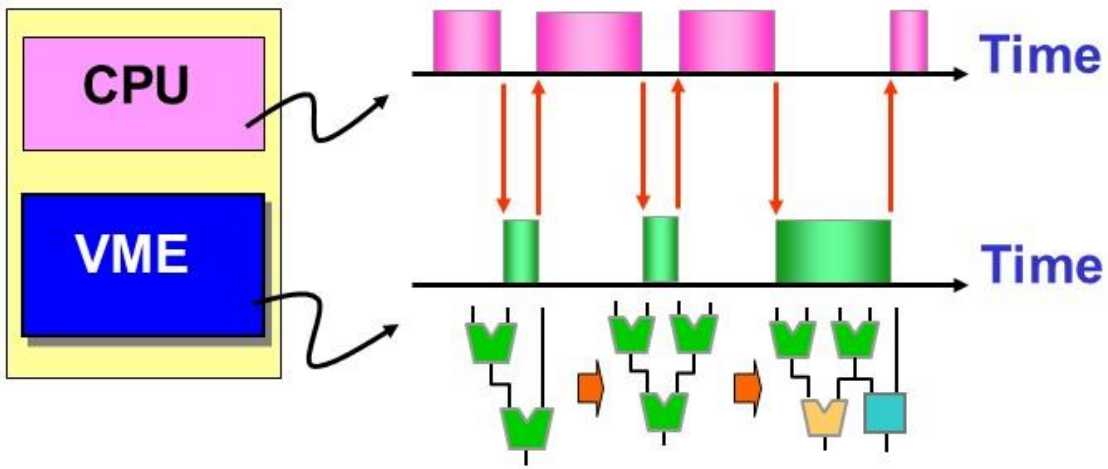


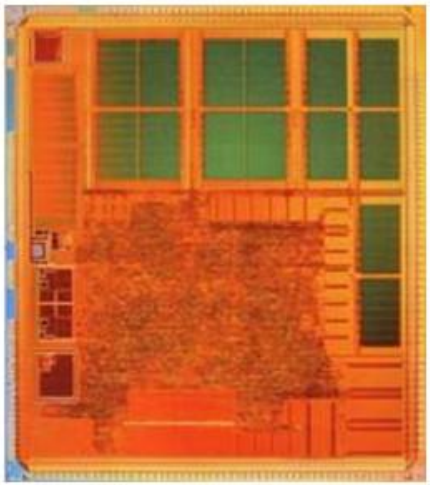
In conventional MPU development, how to raise the performance was the major issue. For future applications, such as mobile products, it is important to improve performance and to reduce power at the same time. In the new RISC MPU, such as SH and ARM, product development along this line is underway. The new generation RISC will become the central core in the post-PC era.



The figure shows the concept of a reconfigurable system. The figure on the left shows a conventional method where different functions (1, 2, 3) are configured by hard-wired method. The right figure is a reconfigurable system where different functions (1, 2, 3) are realized by changing the combination of basic blocks (a, b, c, d). Since only one basic block is needed, power and chip area can be minimized.

Sony's "Virtual Mobile Engine™"





(Logic Function Dynamically Changed)

VME --- a Powerful Engine for Heavier Tasks

CPU with Embedded "Virtual Mobile Engine™"

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As an example of the reconfigurable system, Sony's VME (Virtual Mobile Engine) is introduced. The chip consists of a combination of CPU and VME as shown on the left. The CPU handles ordinary tasks, and VME handles heavy tasks. As shown in the time chart, the configuration of the VME can be changed depending on the task, and heavy task processing can be performed at low power.

World's Smallest Network Walkman

Chip Configuration	One CPU with Embedded *"Virtual Mobile Engine™"*
Decoding Power Dissipation for ATRAC3	Ultra Low Power: 4mW (Less than 1/4 compared to DSP)
Feature	Programmable: ATRAC3/ ATRAC3plus/ MP3

W:36.4mm,H:48.5mm, t:18.0mm

- 11 CDs Recordable
- 33 Hours Non-stop Play
- Storage Media: MagicGate Memory Stick-Duo

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This introduces the world's smallest network Walkman using VME. CPU and VME are integrated on the chip. The power at decoding is 4 mW, which is 1/4 or less than the ordinary DSP processing. Memory capacity is equivalent to 11 CDs, and music can be enjoyed for 33 hours nonstop.

Power Reduction at Algorithmic Level

Vendor	Tool	Features
ASC	PACIFIC	Behavior Synthesis and Power Reduction Based on Input Vector
Chipvision	ORINOCO	Optimizes Memory Access and Date Processing Based on C Code Analysis
Power Escape	Power Escape Analyzer, Power Escape Optimizer	Identifies Memory Access Bottleneck in C Code, then Optimizes Algorithm

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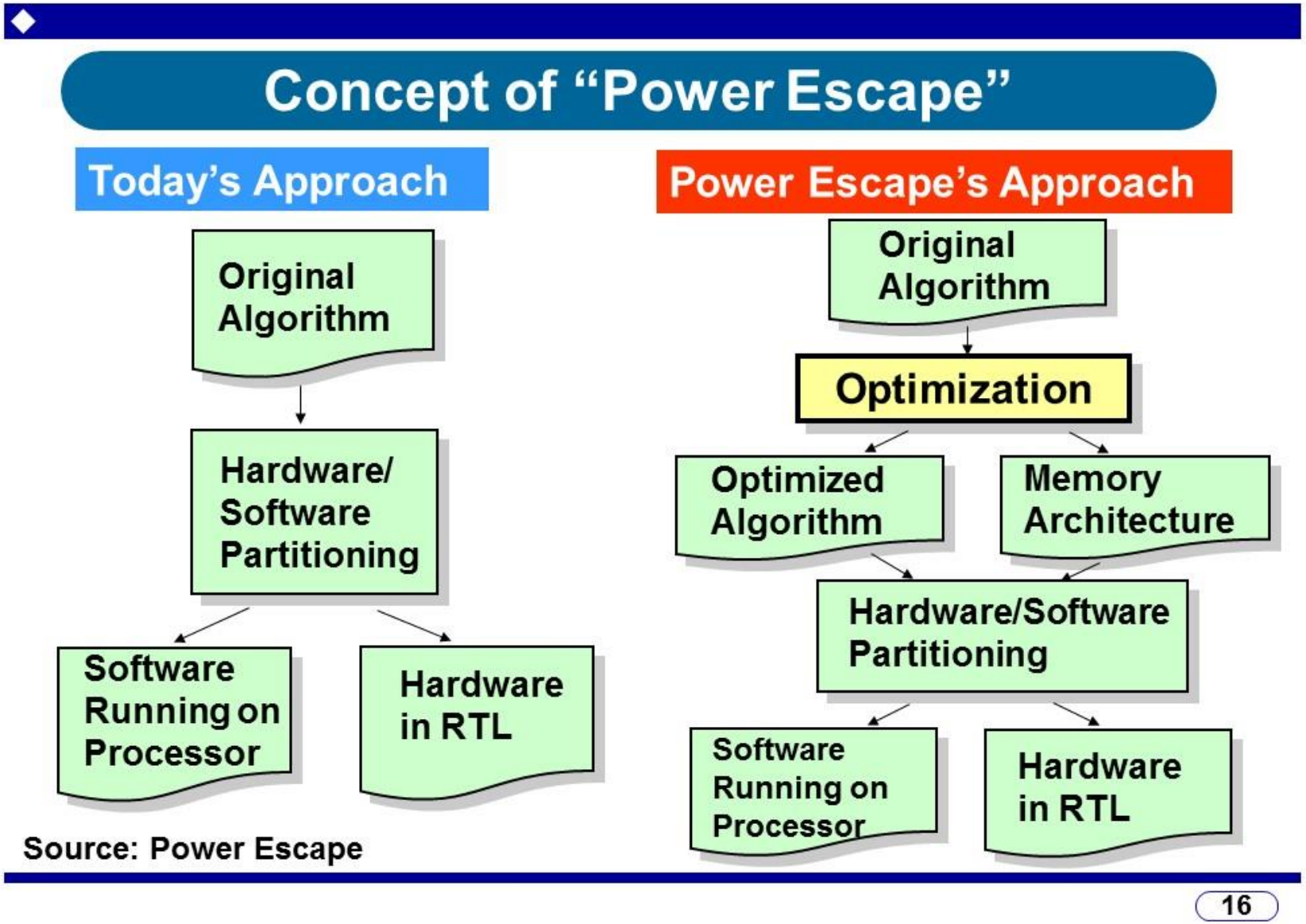
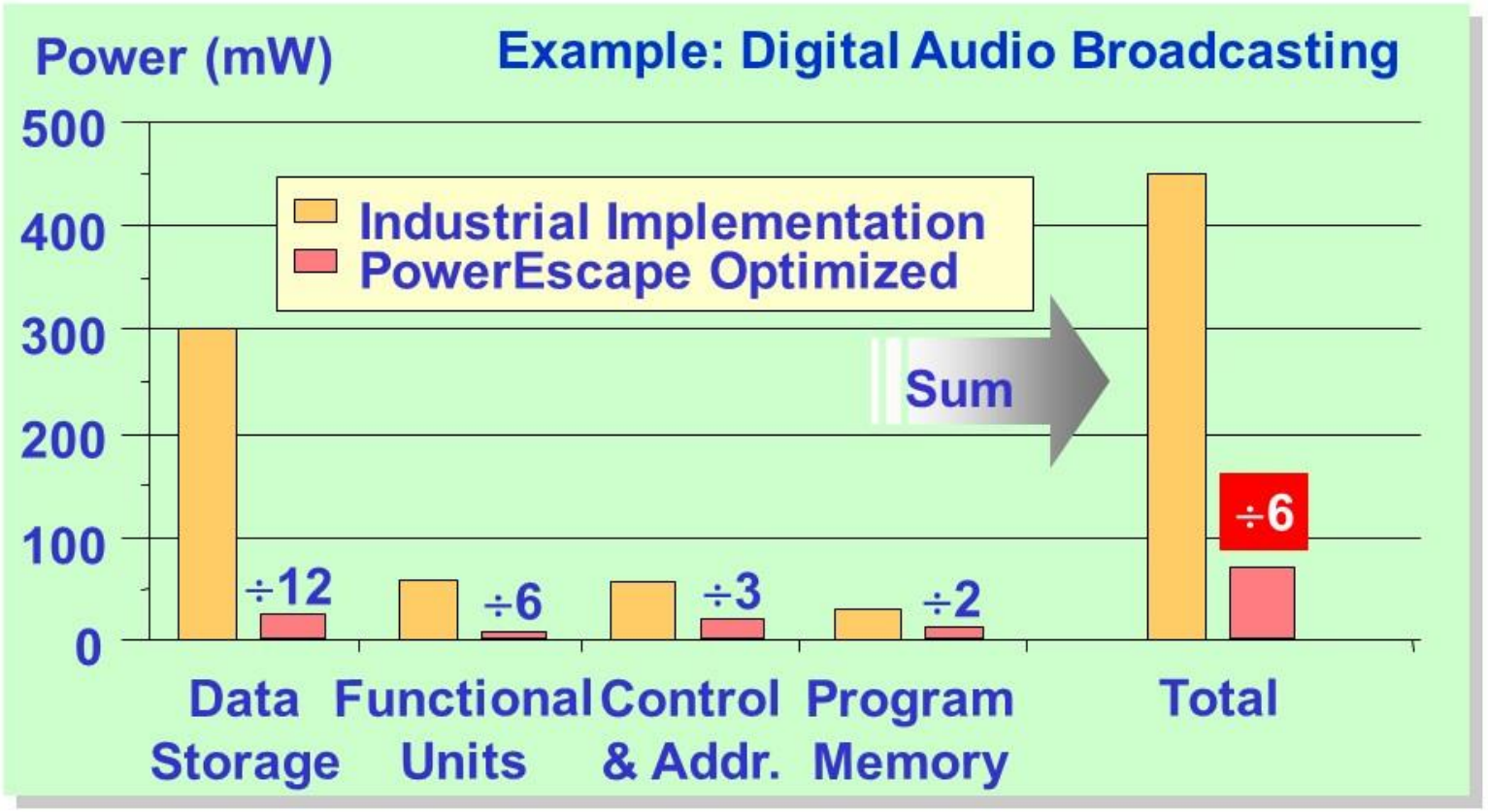
Methods for reducing power on the basis of algorithms have also been developed, and software tools are being sold by ASC, Chipvision, Power Escape and others. The right column shows the main features of each product.



The left is an ordinary design flow of SoC where hardware / software partitioning is performed based on the original algorithm version. On the other hand, in the case of Power Escape on the right, hardware/software partitioning is done after "optimizing" the original version.

Results of "Power Escape" Concept



Source: Power Escape

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This figure shows the effect of "optimizing" by Power Escape software. The left bar chart (brown) is the power consumption when using the original version, and the right (red) is the case when "Optimization" is performed with Power Escape software. As a whole, the power is reduced to 1/6 as shown in the far right. The result shows the significance of algorithm optimization by software.

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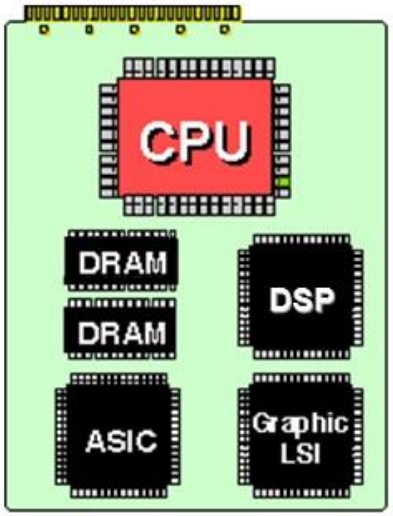
SoC: System on Chip

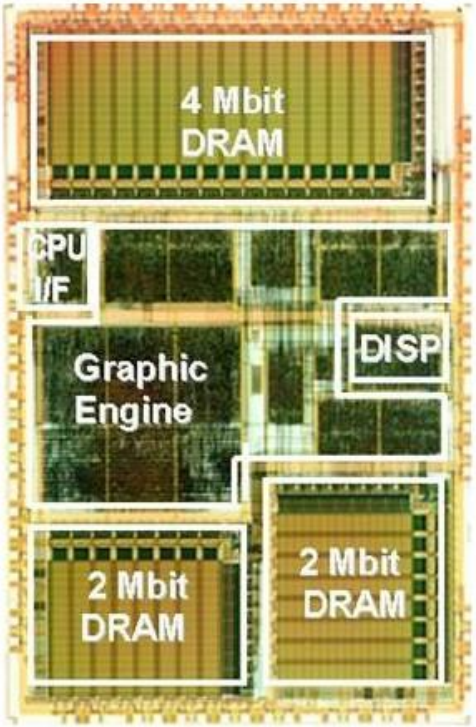
SoB



SoC

3-D Graphics Engine

	SoB	SoC
Performance	x1	x4
Power	x1	x1/5
Chip Counts	x1	x1/4



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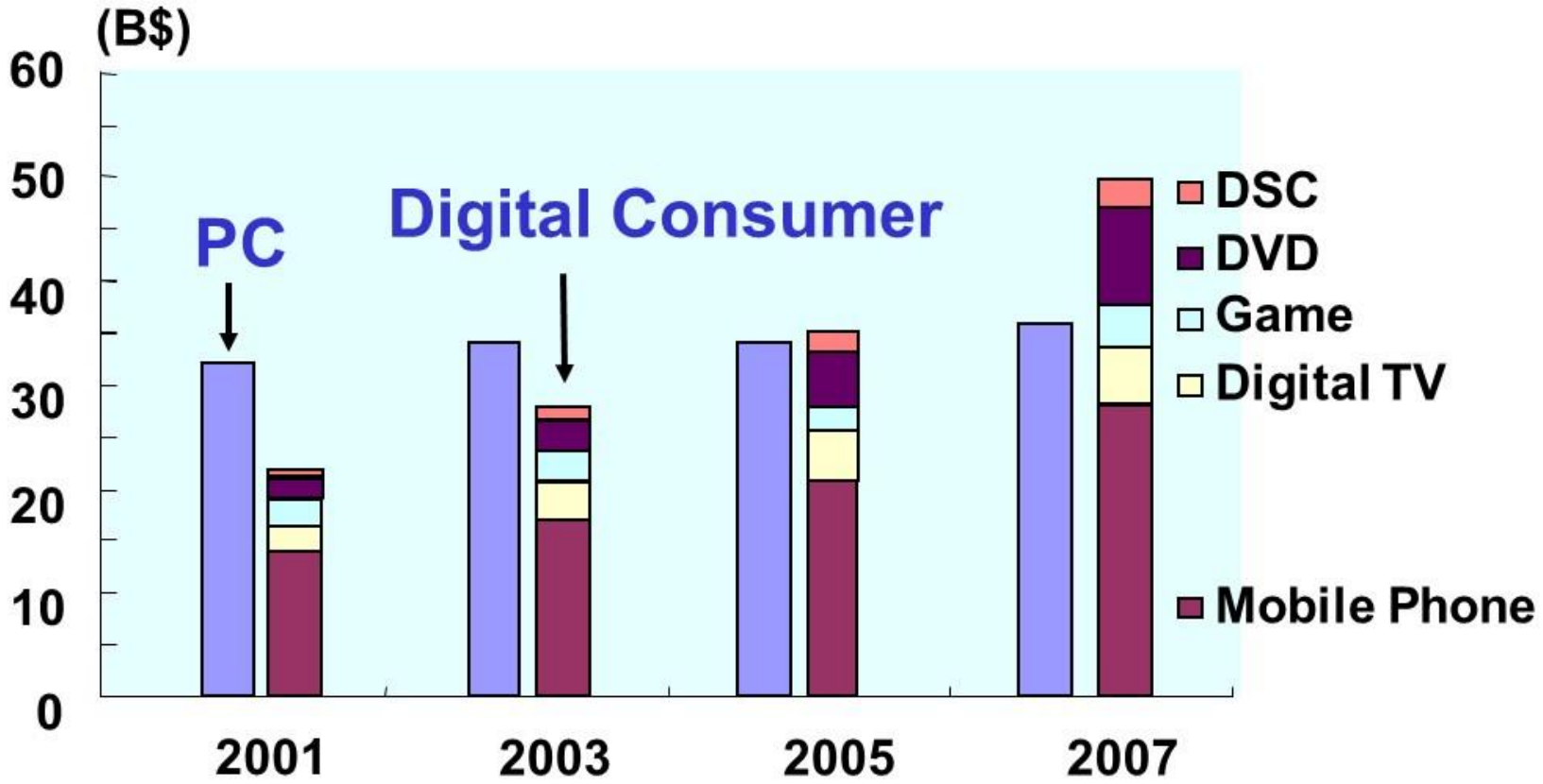
This figure is a comparison between SoB (System on Board) and SoC(System on Chip) of 3D graphic engine. Both have the same function. By shifting from SoB to SoC, the performance is improved by 4 times, the power to 1/5, and the number of chips to 1/4.

Growing Digital Consumer Market



Source: Future Horizons

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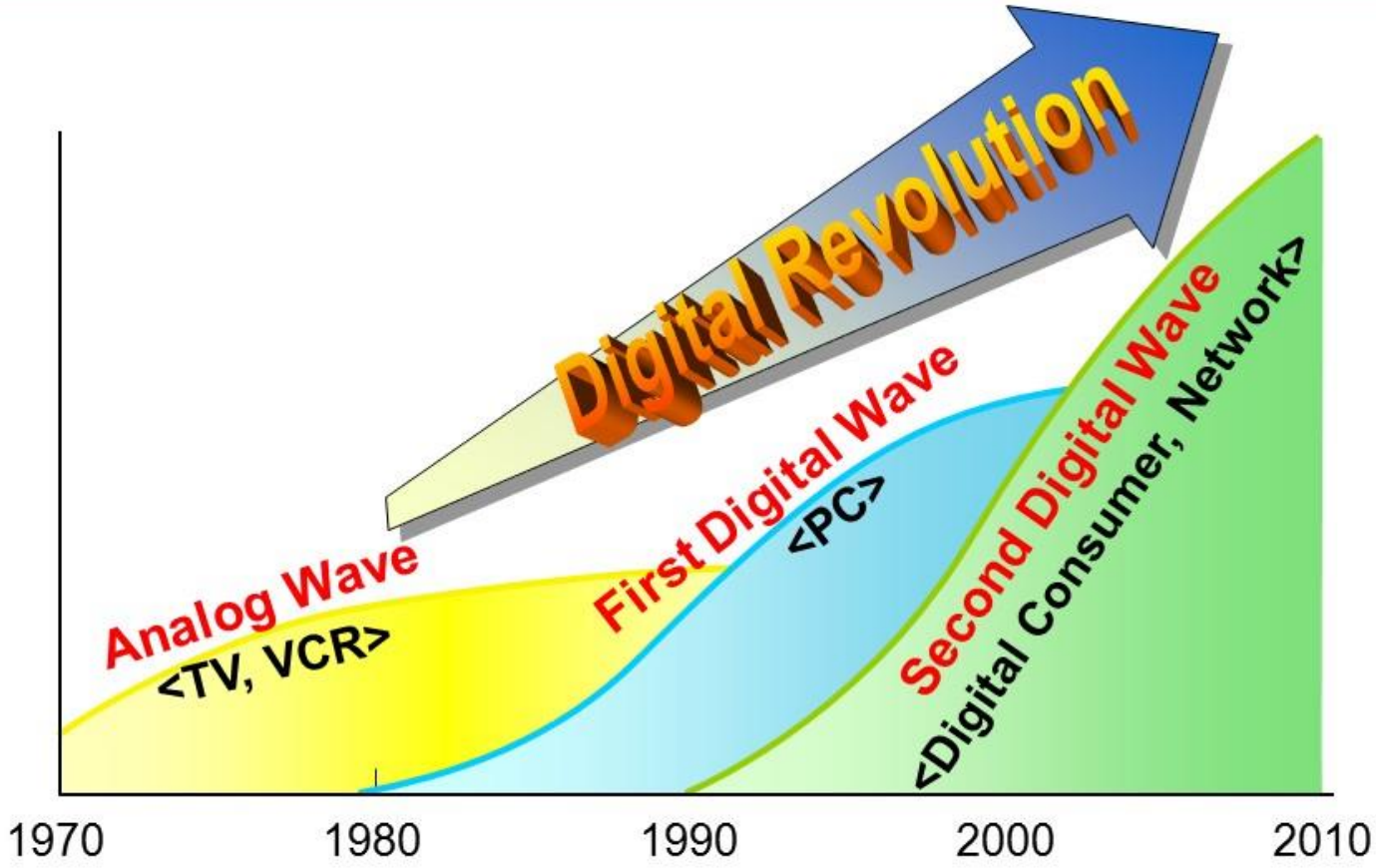
SoC is an indispensable device for digital consumer products, and both SoC and the applied products are growing with synergistic effects. The digital consumer market will surpass the PC market in 2005, centering on mobile phones that need "low power and high performance". It is the digital consumer product that drives the semiconductor market from now on, and SoC is the device that supports it.

Rising Wave of Second Digital Revolution



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The concept of “Second Digital Wave" was introduced three years before this speech, in 2000, predicting it would surpass “First Digital Wave (PC)" by the mid 2000s as shown in the figure. Due to the synergistic effect with SoC, the market is moving in this predicted direction.

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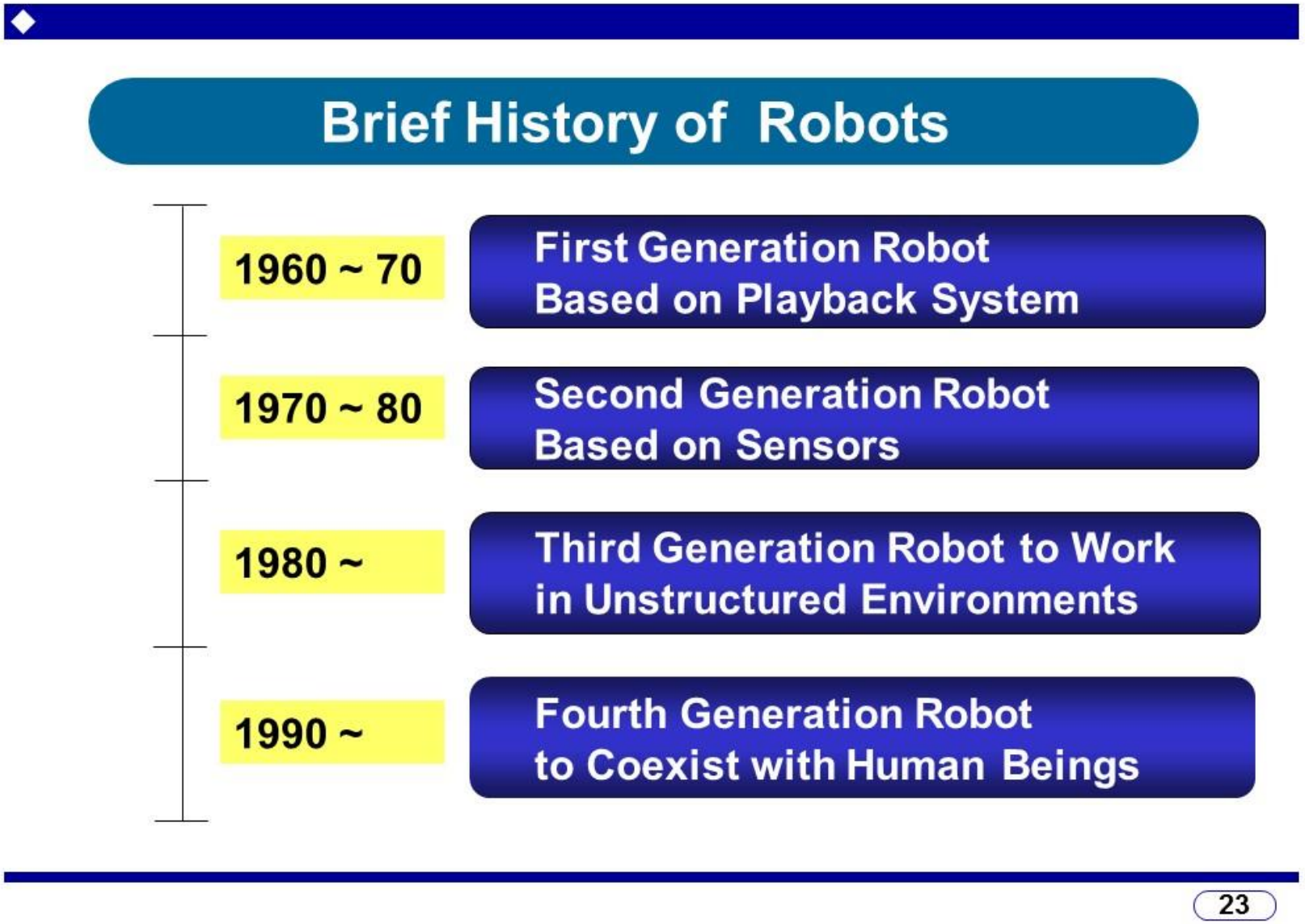

Robots will be the future drivers of low power electronics. Robots have evolved steadily in line with advances in semiconductors; robots based on playback system in the 1960s, sensor based robots in the 1970s, robot working in unstructured environments after the 1980s, and robots coexisting with human beings since the 1990s, and they will further evolve into the future.

Sony's Humanoid Robot

(SDR-3X) (SDR-4X)

- SDR: Sony Dream Robot
- Project Started in 1997
- SDR-3X Demonstrated in 2000
- SDR-4X Demonstrated in 2002

Sony's Biped Robot Pioneers:
T. Ishida(Left) and Y.Kuroki(Right)

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Let me introduce the humanoid robot SDR developed by Sony. SDR stands for Sony Dream Robot. Development began in 1997, SDR 3X was completed in 2000, and SDR 4X in 2002. In addition to walking, running, dancing, talking, it can stand up if it falls down. The leaders of this project are Ishida and Kuroki; alumni of Waseda University.

Chips & Sensors for Robots

VLSI chips

64bit CPU x 3
16bit MCU x 29
DSP x 23
ASIC x 4
FPGA x 3
DRAM 192MB
Flash 16MB

(SDR-4X)

25

The figure shows LSIs and sensors used in SDR4X. In an autonomous robot, it is required to grasp the surrounding situation with sensors in order to make a proper judgment. A total of 79 sensors are used in this robot. The total performance of LSIs is equal to or higher than the PC at that time. Since the robot operates by batteries, low power is essential, and it will lead the future technology.