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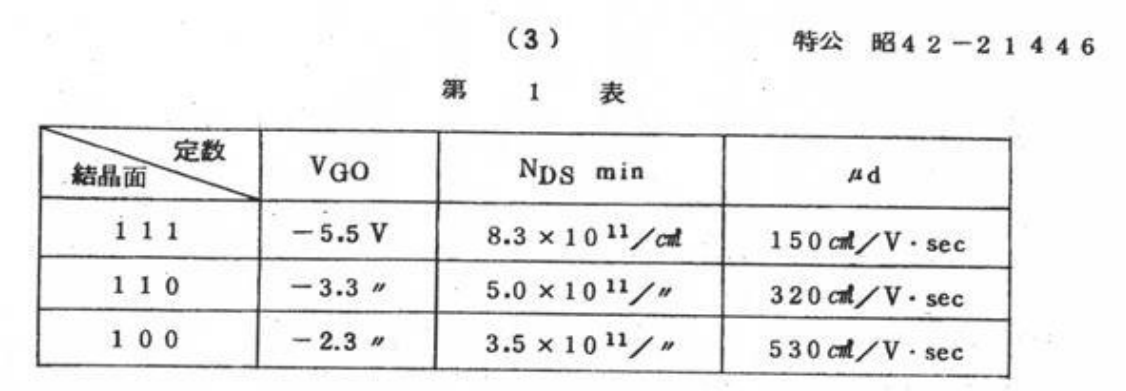
1963

Invention of (100)-plane MOSFET and bias-temperature (BT) treatment technique (Hitachi, Ltd.)

~ Discrete Semiconductor/Others ~

At the time when BTL's Kahng and Atalla succeeded in the operation of a MOSFET for the first time in 1960, its characteristics were unstable and were insufficient for practical applications. The unstable operation was mainly caused by various charges existing in the oxide film and the oxide-silicon interface. The main electric charges are fixed charges due to structural defects of the oxide film, interface states derived from defects at the oxide film-silicon interface, and mobile ions such as sodium, potassium, and hydrogen.
Among these, since the mobile ions moved in the oxide film by an electric field, they were the major causes of unstable operation.

Hitachi's Ohno et al. applied a negative voltage to the gate of a MOSFET and a positive voltage to the source and the drain, heating it at 200-350°C, and then cooling it down, and discovered that mobiles ions were attracted to the gate electrode side and were fixed there, and they named it FC (Field Cooling). They discovered it and filed a patent application in 1963. (Japan Examined Patent Publication No. 41-3418). In 1964, IBM's D. Kerr announced the same operation with the name of B-T treatment (Bias-Temperature Treatment), and the name thereof has been generally used.
As a result of removing the influence of mobile ions, it became possible to measure the crystal plane orientation dependence of the fixed charges and the interface states at the oxide film-silicon interface, and they confirmed <100>surface was more suitable for MOSFETs than <111> surface generally used at the time, and they filed a patent application (JP-B-42-21446). It is a famous <100>crystal surface patent.



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第　1　表

定数 / 結晶面	V_{GO}	N_{DS} min	μd
111	−5.5 V	8.3×10^{11}/cm	150 cm/V・sec
110	−3.3 〃	5.0×10^{11}/〃	320 cm/V・sec
100	−2.3 〃	3.5×10^{11}/〃	530 cm/V・sec

Table 1: Comparison of characteristics of MOSFETs described in patent specification

MOSFETs are fabricated on Si substrates with different crystal planes and compared.
Substrate: p type (specific resistance 100 Ω · cm)
Oxide film thickness: 150 nm
Gate length: 7 μm
The surface donors (ND) (fixed charges and interface levels) are minimum for <100>plane. Therefore, the surface inversion voltage (VGO) is also low. Interfacial dependence is also observed in electron mobility (μd), indicating the superiority of the <100>plane.

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