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Invention of the DSA MOSFET (Electrotechnical Laboratory)

~ Discrete Semiconductor/Others ~

For the high speed and high frequency operation of MOSFET, shortening of the gate length is required. In order to realize high speed and high frequency operation, a short channel gate of 1μm or less is required. However, at the time, the minimum processing size was 5-7μm in the contact lithography era. For this reason, several MOSFET structures that realized a short channel gate by a method other than lithography processing were devised.

Tarui et al. of the Electrotechnical Laboratory devised DSA (Diffusion Self-aligned) MOSFET, by the application of double diffusion technology used for bipolar transistors in which emitter and base were formed simultaneously. In this method, base forming impurity and emitter forming impurity were simultaneously diffused, in the optimized conditions of diffusion coefficient difference, surface concentration difference, diffusion temperature and time. P-type impurity and n-type impurity were diffused from source diffusion window on the n-type substrate, thereby forming p-layer and n-layer (refer to Fig.1). Since the diffusion depth of impurity can be controlled with the accuracy of less than 1μm, MOSFET with much shorter channel length than the one fabricated by lithography method could be made. It came to be called D-MOS (Double-diffused MOS Transistor) at IEEE.

Tarui et al. observed high-speed switching with tp=1.2ns (tpp=2.5pJ) in a submicron channel E-D DSAMOS FET ring oscillator. Furthermore, H. J. Sigg et al. of Signetics realized a DSAMOS FET with a channel length of 1.3μm, f_{max}=10GHz, gain=7dB (at 2GHz). It was a revolutionary value at that time. High speed operation of the DSAMOS FET was greatly expected as a logic LSI and the development was promoted. Mitsubishi Electric's Tomizawa et al. developed a 920 gate E-D type master slice and realized an operation speed of 3ns. However, after that, as the lithography technology advanced and CMOS emerged, the superiority of DSAMOS was lost. Rather, by the characteristics of DSAMOS suitable for high-voltage operation, it has developed as a power MOSFET. Recently, SiC DMOS FET with 1200 V breakdown voltage has been developed.

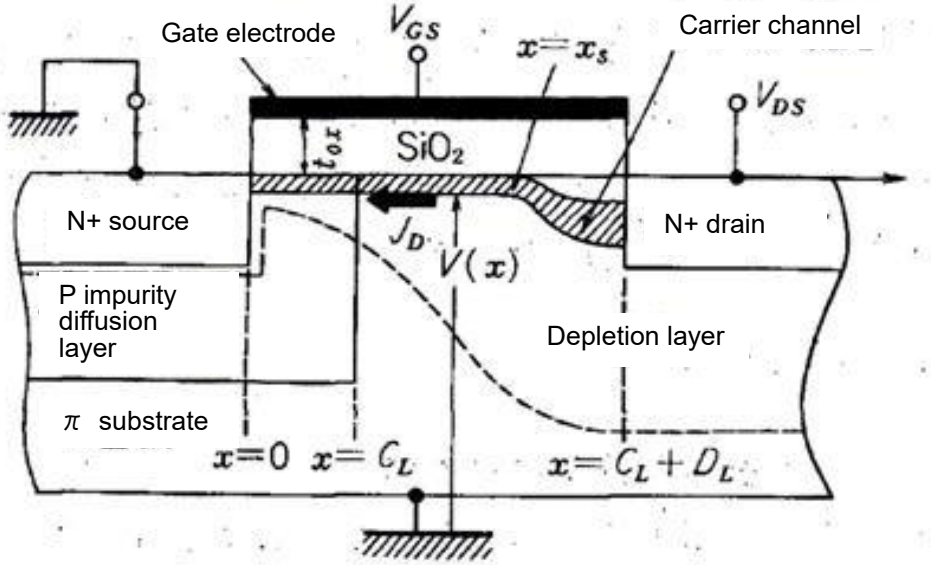

図1　πプレーナ形DSA-MOSトランジスタの断面模型図

Fig.1－Schematic cross section of π planar DSA-MOS transistor.

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