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Late 1950s
Vapor diffusion source and diffusion furnace
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For the formation of the diffusion layers of the initial transistors, solid phase diffusion method was used, using solid materials such as P_2O_5 or Sb_2O_5 for n type and B_2O_3 or Ga_2O_3 for p type. However, with this method, defects due to local aggregation of the diffusion source were likely to occur, and it was unstable to form a thin base layer to enhance high frequency characteristics. In 1957, Carl Frosch and Lincoln Derick of Bell Telephone Laboratories developed a method of vapor phase diffusion with the silicon oxide film as the mask, using gases such as $POCl_3$ and B2H6 in the electric furnaces (horizontal diffusion furnace) [1].

The thermal oxidation method of the silicon oxide film used as the diffusion mask was born by an accident of hydrogen explosion during the development of vapor phase diffusion method. Oxide film was formed on the silicon surface by H_2O generated by the explosion. Hereafter, the thermal oxidation method by the horizontal diffusion furnace has been used.

In 1959, Jean Hoerni of Fairchild Semiconductor developed the planar process by the enhancement of this gas phase diffusion method [2], and in that same year Jay Last and Robert Noyce applied step-and-repeat photolithography technology and reached the invention of planar integrated circuit technology.

References:

【1】Computer History Museum, “Development of Oxide Masking”

【2】Computer History Museum, “Invention of the planar manufacturing process”

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