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First half of the 2000s
Rapid heating/cooling vertical furnace
~ Discrete Semiconductor/Others ~

Horizontal furnaces had been used for the heat treatment processes of oxidation, diffusion and film deposition such as LP-CVD from the early days of semiconductor fabrication, and were replaced by vertical furnaces in the 1980s. Both horizontal and vertical furnaces performed batch processing in which around 100 wafers were placed in a quartz furnace and all wafers were isothermally heat-treated. In this method, (1) waiting time was required until wafers were prepared in units of 100 wafers, and (2) long time was required for temperature rise and fall due to the large thermal capacity.
In the 1990s, system-on-chip (SoC) LSIs which were diverse by its nature, became dominant, and small-volume production of a wide-variety of SoC products increased. And then, waiting time (1) became the issue to reduce production turnaround time.
In addition, the long rise and fall time (Thermal Budget) in (2) became an obstacle to make the diffusion depth shallow. This problem became apparent especially in the activation process of the ion implantation layer, and the furnaces ware replaced by single-wafer lamp annealing systems with shorter heating and cooling times in the late 1990s. Mainly because of these two points, even in the deposition process, expectations were raised for single-wafer thermal processing equipment. In the end of the 1990s, fabs that performed all of deposition and heat treatment processes in single-wafer system emerged.

On the other hand, it was necessary to increase deposition speed to improve productivity especially from the aspect of single-wafer deposition. Fast deposition performed in supply rate-controlling region of reaction gas, but in this region, the film thickness had a tendency to be affected by means of the film pattern density. Film deposition rate of vertical furnaces which were operated in the surface-reaction rate-controlling region was lower. However, this method increased productivity by means of batch processing of 100 wafers. At the same time, it was possible to deposit a film with uniform thickness independently of pattern density unevenness on the wafer surface. In 2001, Tokyo Electron developed a rapid heating and cooling vertical furnace (TEL FORMULA) that overcame the obstacles (1) and (2), utilizing these features.
The furnace had a batch size of 25 wafers. In addition, the time required for temperature rise and fall was significantly reduced by using a metal heater which was capable of generating heat at high temperatures, and further lowering of the heat capacity of the furnace body. Required time for most oxidation and LPCVD deposition processes, which was previously 4-5 hours, was reduced to around 1 hour. In 2002, Hitachi Kokusai Electric (later Kokusai Electric) adopted the fast heating and cooling system in its 100-batch vertical furnace (QUIXACE). This fast temperature rise and fall system became the standard for vertical furnaces. Rapid heating/cooling vertical furnaces and single-wafer systems

were chosen respectively depending upon wafer processing requirements.

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