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2005
Cell Broadband Engine
(group consisting of Toshiba, IBM, and Sony Corporation)
~ Integrated Circuit ~

(Cell Broadband Engine)™ (Cell/B.E.™) is a multi-core processor jointly developed by Sony Computer Entertainment, Sony Corporation, IBM, and Toshiba. Starting from the summer of 2000, they began studying with the goal of realizing processing performance of 100 to 1000 times that of PlayStation 2, which was just developed at the time. In March 2001, four companies opened STI Design Center in IBM's development center in Austin, Texas, USA, and gathered engineers and started the full-fledged development. And in February 2005, details were announced at ISSCC.
In architecture design, in order to cover from home game machines to supercomputers, it was required to satisfy "three P", namely "high performance (Performance)", low power consumption (Power) and “low price (Price)”. The most significant feature for realizing this is the adoption of an asymmetric multi-core configuration.

At the time of the development start, an architecture of a single processor operating with a high-speed clock was mainstream, as typified by Intel's Pentium 4 processor, and it was generally thought that the clock frequency would continue to improve until around 2010. However, the increase in power consumption accompanying the improvement of the clock frequency became a problem, and thereafter mass production of processors with clock frequencies exceeding 4 GHz did not appear except for server processors that could use large-scale cooling devices. In Cell/B.E., in order to maximize the performance per transistor number, they adopted a multicore configuration consisting of a total of nine processors, each of which was a simplified processor core, as a vanguard of multicore design.

In addition, in Cell/BE, in order to satisfy "three P" to the maximum extent, an asymmetric multicore configuration was adopted, consisting of one PPE (Power Processor Element) which was a general-purpose processor and 8 SPEs (Synergistic Processor Elements) for which a new architecture was defined for flexible implementation of advanced real time multi-media processing.
The general-purpose microprocessor PPE controls the total system. By adopting a 64-bit PowerPC architecture that had been proven in a wide range of applications ranging from embedded applications to high-performance servers, it has made it possible to reuse huge software assets including OS and development environment. In its implementation, a micro architecture with high area and power consumption efficiency is adopted.

On the other hand, SPE adopted a new architecture pursuing high data processing performance and multimedia computing performance. Based on the premise of coexistence with PPE, bold architecture

selection which was not restricted by software compatibility became possible. The SPE is a processor for data processing of 128bit SIMD (Single Instruction / Multiple Data) type and consists of a Synergistic Processor Unit (SPU) and an advanced function DMA (Direct Memory Access) controller MFC (Memory Flow Controller).

One characteristic of SPE is the adoption of internal memory called local storage (LS) instead of cache memory. Instruction fetch and data access of the SPU are performed only for this LS, and data transfer with the outside of the SPE such as the main memory is performed only by the DMA of the MFC. Since cache miss and address translation error do not occur from SPU, fixed access latency is guaranteed, realization of real time property is made easy. By concurrent program execution and DMA transfer, it is possible to conceal memory access latency of several hundred cycles. In addition, a micro architecture putting emphasis on area and power efficiency such as large-capacity register file of 128 bits×128 lines, software branch prediction, etc. is adopted.

Cell/B.E. was installed in Sony Computer Entertainment's game machine PlayStation 3, and was later adopted by Toshiba's digital TV (<CELL REGZA>). In addition, as a derivative product of Cell/BE, Toshiba developed the media streaming processor SpursEngine which installed 4 SPEs and a hardware dedicated to video encoding and decoding (announced in September 2007), and adopted it in the company's notebook PC. IBM also developed the PowerXCell 8i processor with enhanced double precision floating point arithmetic performance (announced in May 2008), and adopted it in the world's fastest (TOP 500 (R) as of June 2009), supercomputer Roadrunner etc.

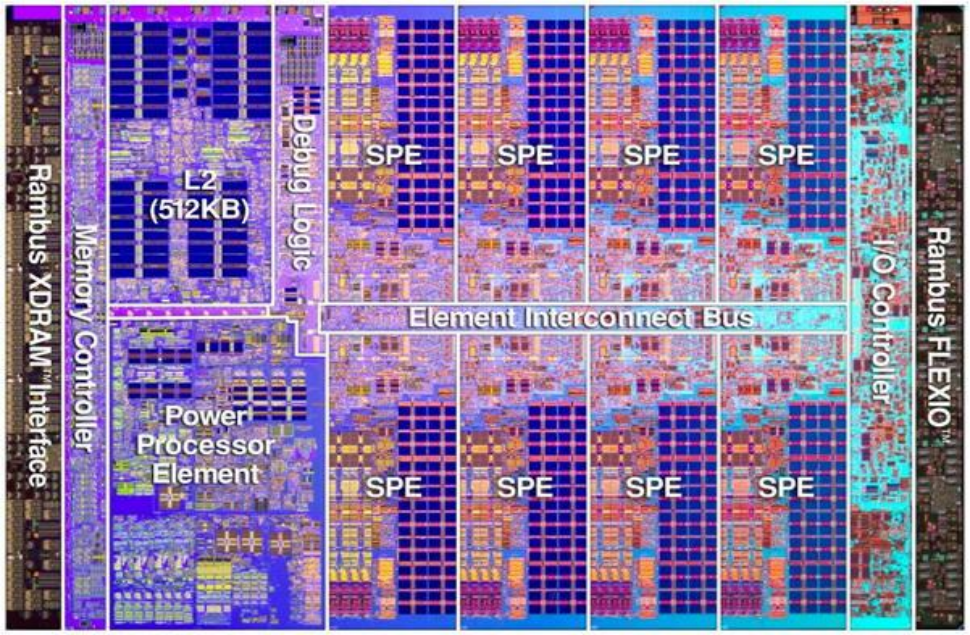

Figure: Die photo of Cell chip (By courtesy of Toshiba)

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