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2015
TSV Stacked DRAM (Hynix, Micron)
~ Packaging ~

HBM is a high-bandwidth DRAM that stacks memory chips three-dimensionally using through-silicon-via (TSV) technology standardized by JEDEC in 2013. By connecting the host processor (GPU/CPU/SoC, etc.) with bus bandwidth of 1024 bit per stacked HBM module, broadband and low power consumption can be achieved. As the method of connecting with wide bus width, there is a method (3D) in which a TSV is formed on a host processor and connected to the sacked memory module, and another method (2.5D) in which the connection is done side-by-side by using Si interposer. In 2015, AMD launched the GPU “Fisi” with Hynix’s HBM. It is the world first product for consumer use that adopted TSV technology. Fisi consists of a GPU chip and four HBM stacked modules on a Si interposer in 2.5D integration.

In each HBM module, 4 HBM chips of 2 Gbit each are stacked on a chip called base logic in the bottom layer, and they are connected by TSV. The memory capacity per HBM stacked module is 1 GB, and the entire GPU package has 4 GB memory. Also, each HBM stacked module and GPU chip are connected with bus width of 1,024 bits, which makes up bus width of 4,096 bits for a GPU. The transfer rate per lane is 1 Gbit/s, and the total memory bandwidth is 512 GB/s. Furthermore, in the second generation “HBM-2”, the transfer rate per lane becomes 2 Gbit/s, and it is planned to realize the memory bandwidth of 1 TB/s in total.

Meanwhile, HMC is a standard proposed by Hybrid Memory Cube Consortium led by Micron and Samsung as a wideband memory for HPC, and a logic IC with a high-speed transceiver is placed at the bottom layer under the TSV stacked memory. Unlike the HBM’s wide bus connection, the connection with the host processor is a high-speed serial link of 10 Gbit/s per lane. This is characterized by reduction in the number of wirings per memory cube, and long distance between the host processor and memory modules is made possible. Fujitsu announced the super computer “PRIMEHPC FX 100” which adopted this HMC in 2014. The memory bandwidth per processor is 480 GB/s.

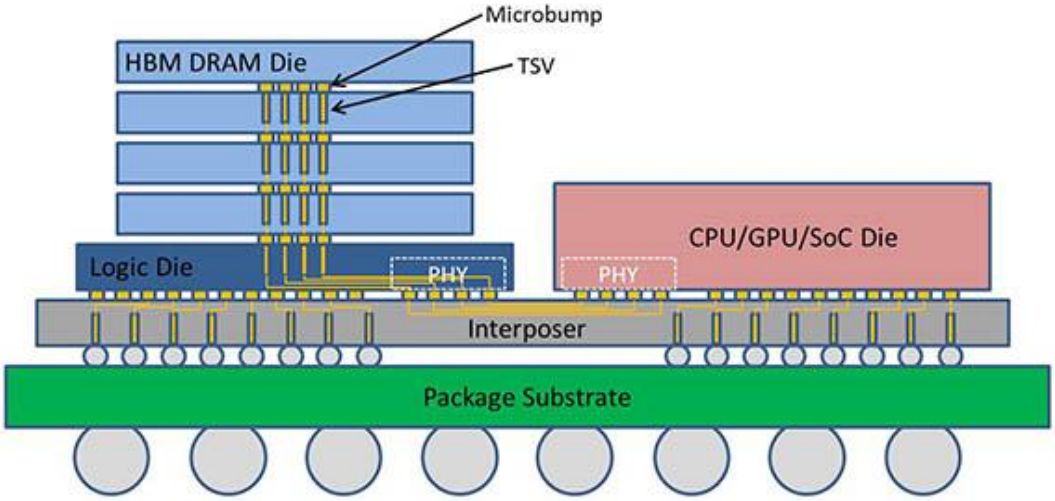

Fig.1 : Structure of HMB

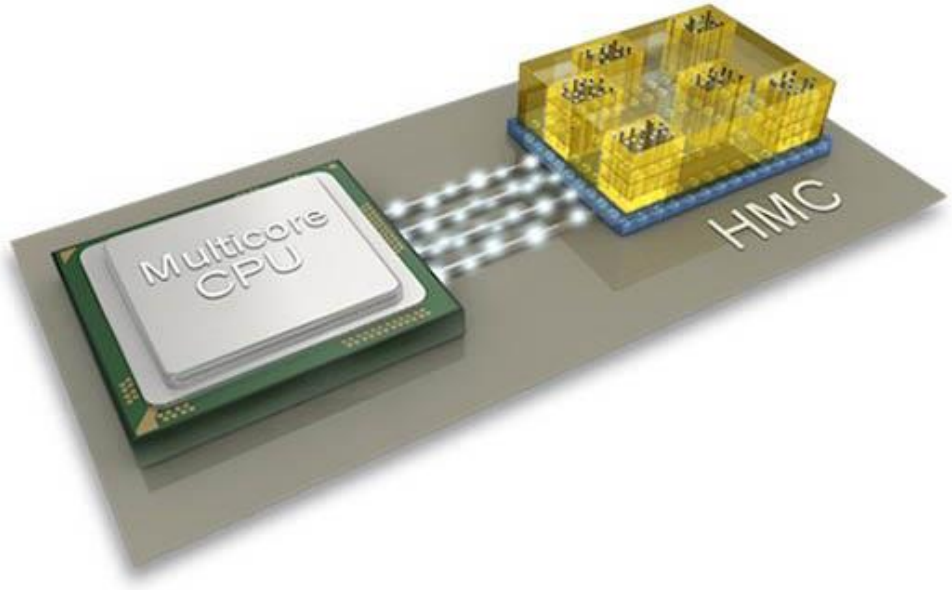

Fig.2 : Image of serial link between HMC and processor
(By courtesy of Micron Technology, Inc.)

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