To search page

2015

Active Development of FOWLP (Fan-Out Wafer Level Package) Technology (Infineon, TSMC, other companies)

~ Packaging ~

FOWLP (Fan-Out Wafer Level Package) is a package having a structure in which a fine redistribution layer (RDL : Redistribution Layer) on an LSI chip is formed extending outwardly from the chip. It is possible to realize high-density wiring between multiple chips and substantial reduction in size and thickness as compared with conventional packages. Miniaturization is realized by applying the thin film process for the wiring processes which is used for the wiring on the conventional silicon wafer processing.

Although TSV (Through Silicon Via) technology is expected as high-density connection technology between chips, especially as a technology for wideband memory connection to processors, at present, high added cost is a bottleneck and its application is limited to some HPC (High Performance Computing) applications. Meanwhile, FOWLP (Fan-Out Wafer Level Package) was licensed to OSAT (Outsource Assembly and Test) companies such as Infineon's "eWLB" (embedded Wafer Level Ball Grid Array) in the latter half of the 2000's, but due to its technical constraints, it has been limited to application to some high-frequency ICs, baseband chips and the like.

Since around 2014, however, movements towards more advanced chip applications became apparent by overcoming FOWLP's technology constraints, and it was reported in the media in 2015 that TSMC's "InFO (Integrated Fan-Out)", a type of FOWLP, would be adopted by Apple's iPhone application processor. In eWLB, the RDL formation was performed on a resin wafer in which a chip called a reconfigured wafer was embedded, whereas in InFO, alignment precision of the chip and rewiring was improved by processing the RDL formation on the wafer, enabling its application to LSIs such as application processors with many terminals. The application to mobile products, which is a huge market of electronics, is thought to be a major driving force for FOWLP's market expansion and technology generalization.Its development is actively carried out as a high density assembly technology that can be applied to high end products which were considered to be covered by TSV technology, with the market participation of foundries, OSAT (Outsourced Semiconductor Assembly and Test) and equipment / material manufacturers.

Research and development of different types of FOWLP technology were conducted in Japan, too, in the 2000's at the same time as eWLB etc. It is a FOWLP technology in RDS-1st method by NEC / NEC Electronics / Renesas Electronics, and it is characterized by its capability of further miniaturization of RDL and combination with TSV stacking technology, unlike eWLB and Chip-1st method of InFO.

The RDS-1st method is expected as a next-generation FOWLP technology, and the development is being carried out at many companies.

Fig.1 : External appearance of FOWLP (By courtesy of ASE)

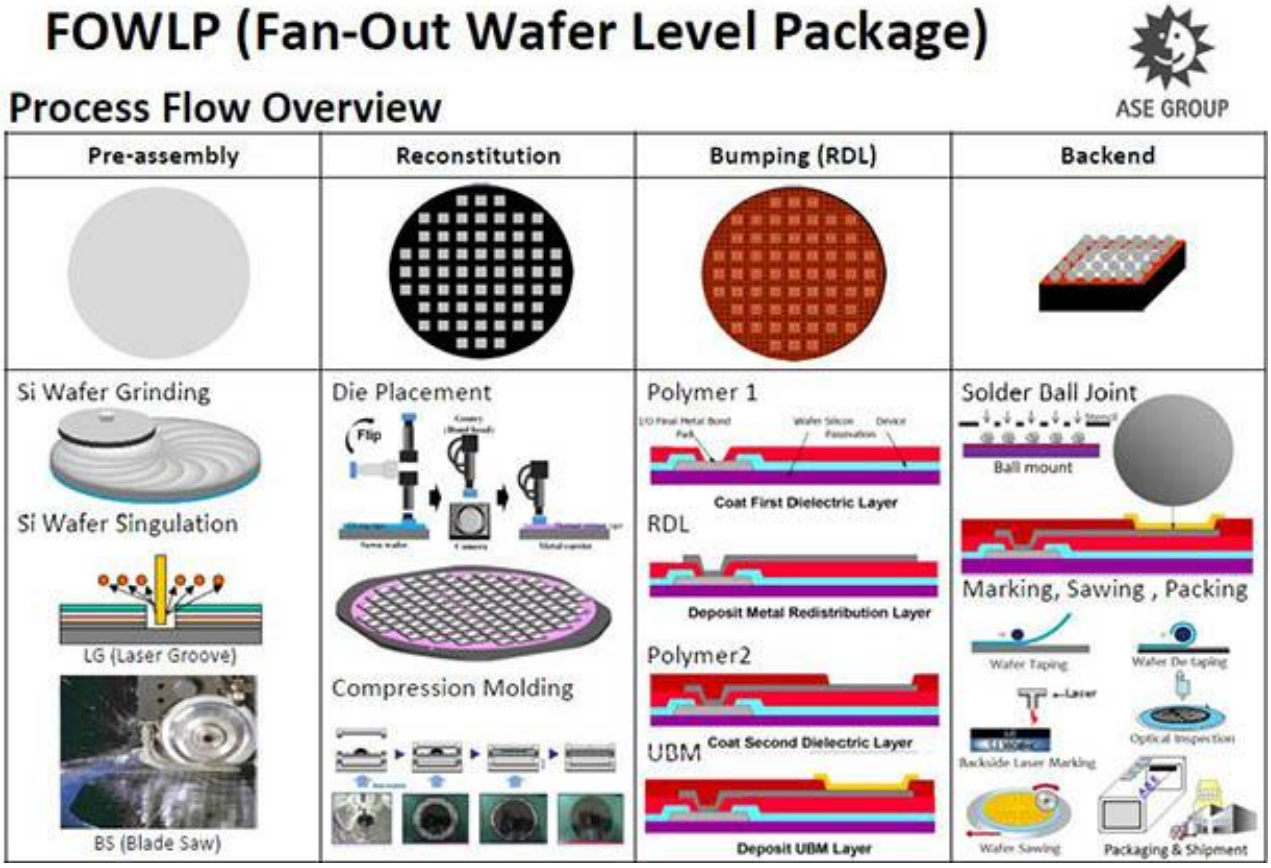

Fig.2 : General process flow of Chip-1st type FOWLP (By courtesy of ASE)

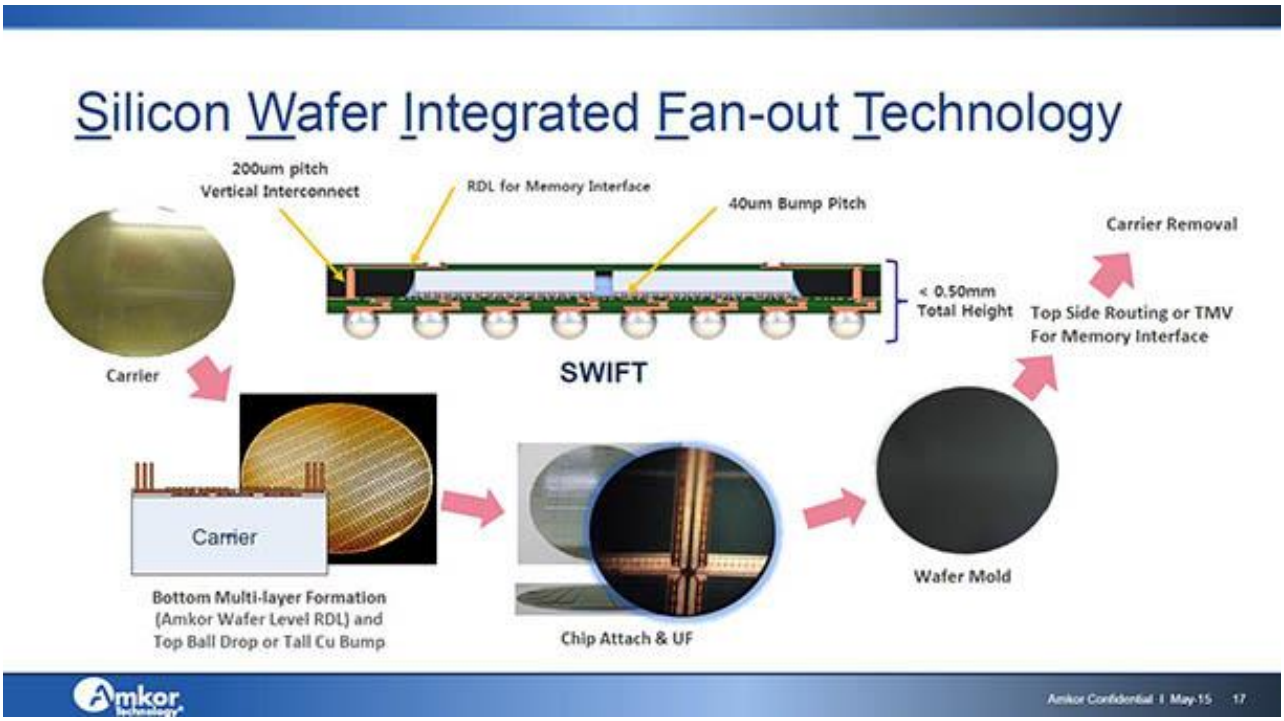

Fig.3 : Example of RDL-1st type FOWLP (By courtesy of Amkor)

Version 2019/1/31