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2015

Inter-chip Wireless Connection Technology TCI (Keio University)

~ Packaging ~

TSV (Through Silicon Via) technology is expected as a means to connect a large capacity / wideband memory with high-speed logic such as a processor, but cost has become an issue, and at the present time it is applied to some HPC (High Performance Computing) applications. Therefore, research and development of techniques for realizing low-cost high-speed chip-to-chip connection at the same level as TSV by using different means are actively conducted. TCI (Thru-Chip Interface) is a technology for wireless chip-to-chip connection that transfers information by a magnetic field generated by passing a current through a coil provided on a stacked chip.

It was proposed and developed by Professor Tadahiro Kuroda of Keio University et al. Processes such as etching of the Si substrate, embedding of conductor vias, and connection between chips by bumps required for TSV stacking are unnecessary and reduction in manufacturing cost can be expected.

In addition, the transmission speed per coil is 40 Gbit/s or more, and the transmission bandwidth per chip area can be as good as TSV. In order to reduce the coil area, it is important to reduce the distance between the superimposed coils, that is, to thin the chip, and research is currently being conducted to laminate chips with a thickness of 4 μm. Techniques for stacking DRAMs and applying them to supercomputers using this technology are also advanced by PEZY Computing, Ultra Memory. TCI is expected to be used as a low-cost chip-to-chip connection technology without mechanical connection, for various applications which are not limited to chip stacking alone, and it will be used as a general technology for chip-to-chip connection in the future.

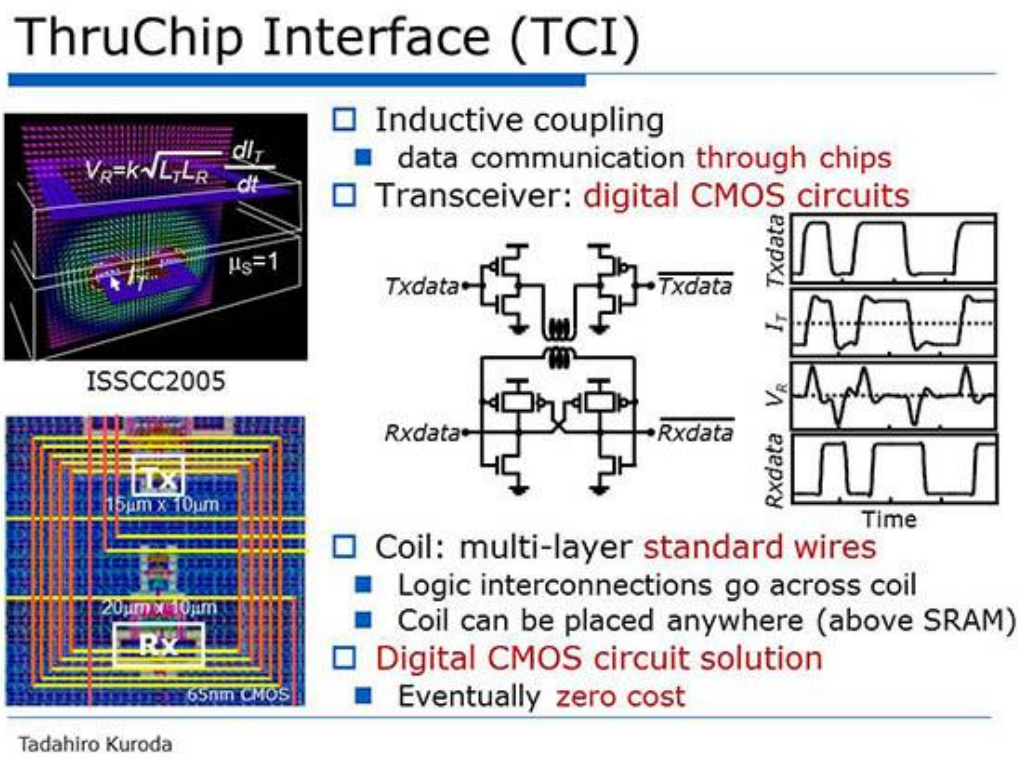


Figure 1 : TCI principle (provided by Professor Tadahiro Kuroda, Keio University)

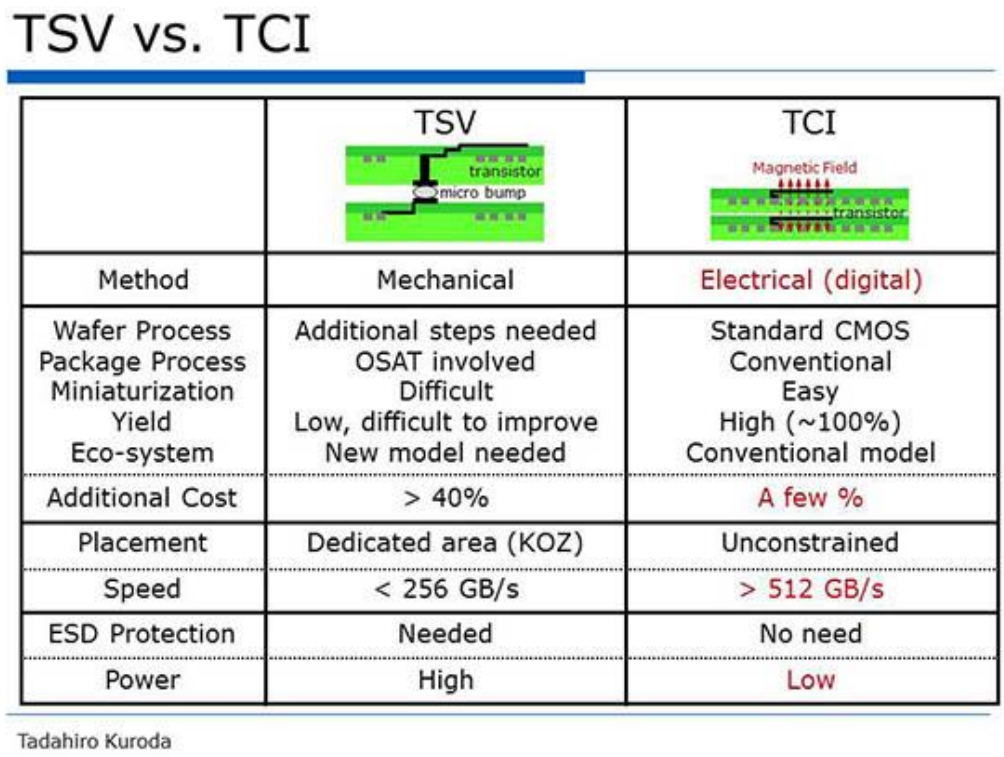
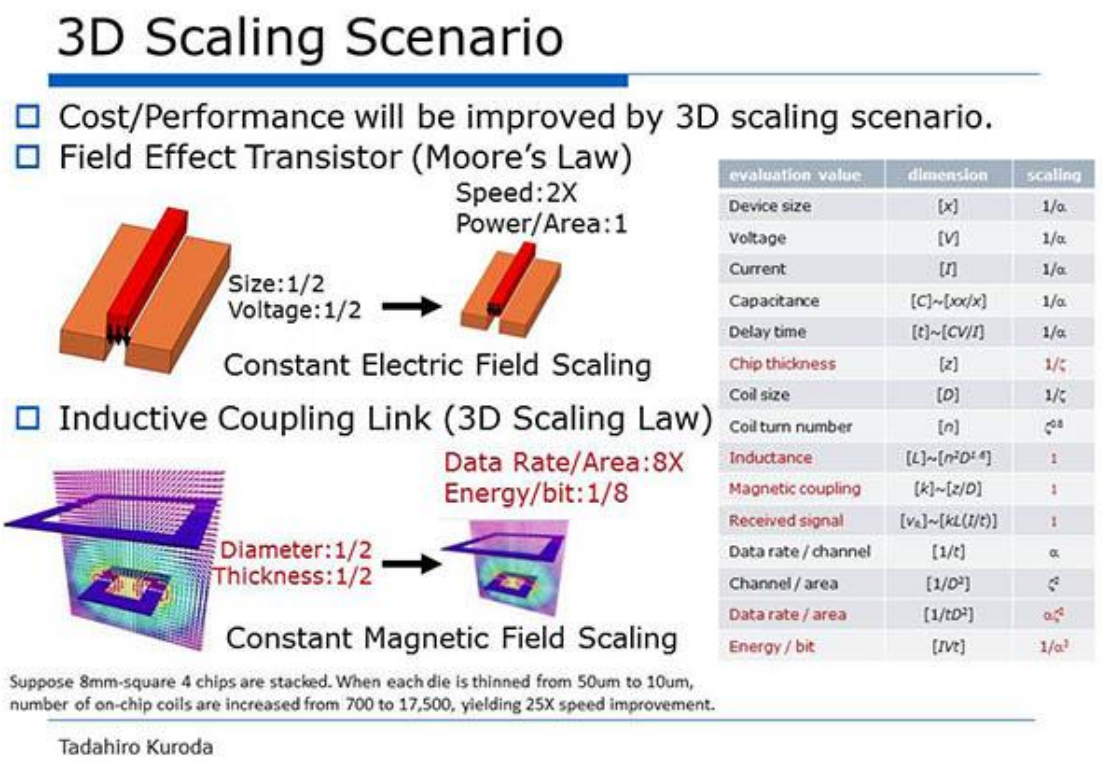


Figure 2 : Comparison of TSV and TCI (provided by Professor Tadahiro Kuroda of Keio University)



evaluation value	dimension	scaling
Device size	[x]	1/α
Voltage	[V]	1/α
Current	[I]	1/α
Capacitance	[C]~[xx/x]	1/α
Delay time	[t]~[CV/I]	1/α
Chip thickness	[z]	1/ζ
Coil size	[D]	1/ζ
Coil turn number	[n]	$\zeta^{0.8}$
Inductance	$[L]\sim[n^2D^{1.4}]$	1
Magnetic coupling	[k]~[z/D]	1
Received signal	$[v_R]\sim[kL(I/t)]$	1
Data rate / channel	[1/t]	α
Channel / area	$[1/D^2]$	ζ^2
Data rate / area	$[1/tD^2]$	$\alpha\zeta^2$
Energy / bit	[IVt]	$1/\alpha^3$

Figure 3 : Evolution of TCI by scaling (provided by Professor Tadahiro Kuroda of Keio University)

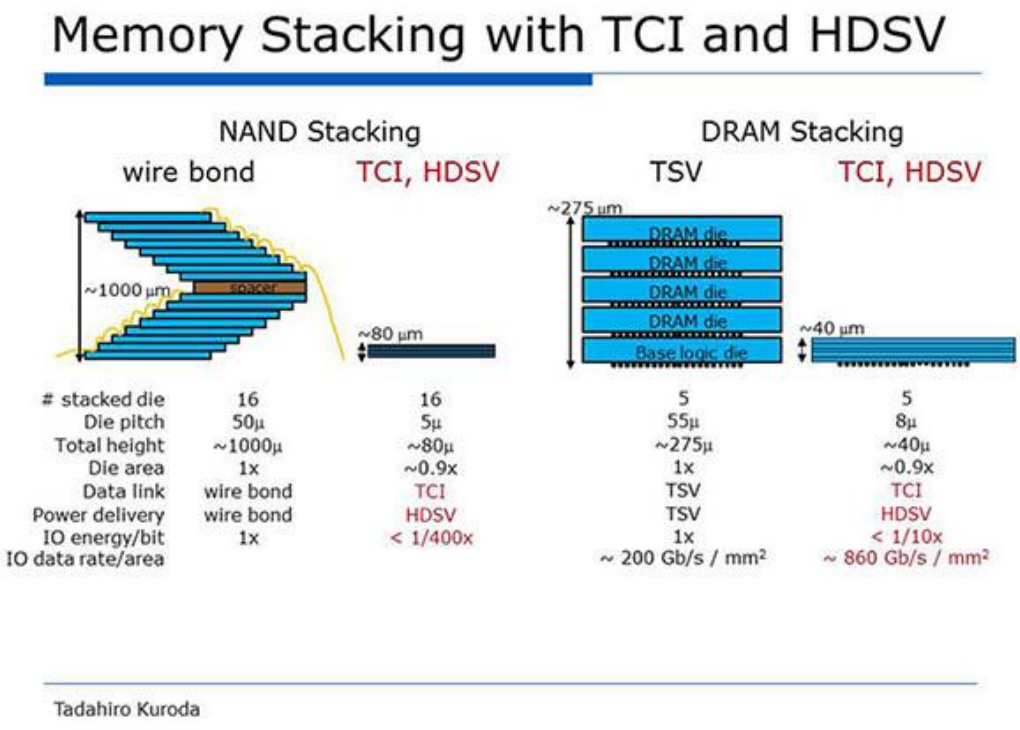


Figure 4 : Large-capacity stacked memory with TCI
(provided by Professor Tadahiro Kuroda, Keio University)

Version 2019/1/31