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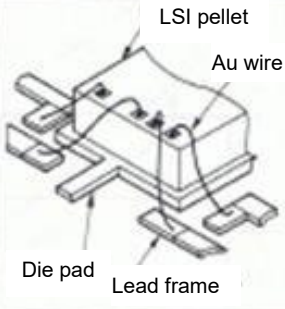
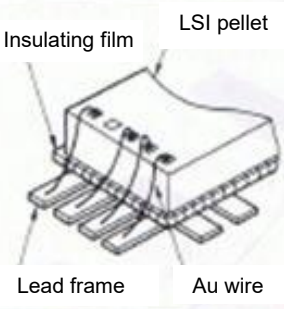
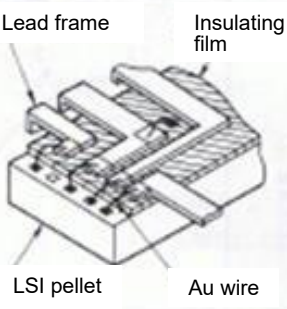
1988
Start of LOC structure development
~ Packaging ~

In 1988, Hitachi announced its activity of LOC (Chip On Lead) technoogy development as a high density packaging technology for DRAM in the May issue of the Nikkei Microdevice, and explained the outline of the technology in August in the same year in Hitachi Review.

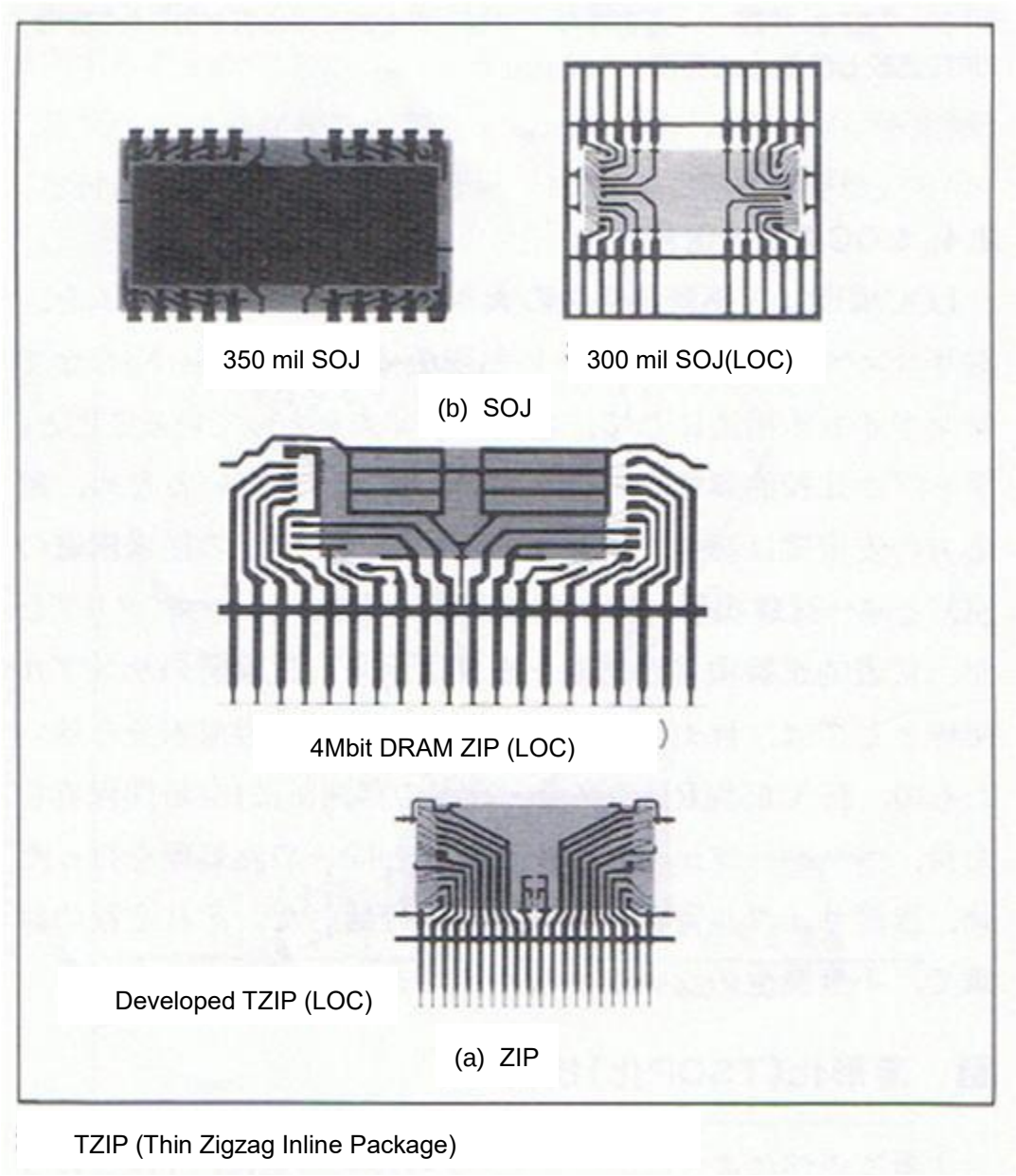
The LOC structure was put to practical use test in SOJ and ZIP (Zigzag In-line Package) of 4 MDRAM, as it could store larger die size component in the same small package outline, and was superior in environmental reliability and electrical characteristics as well, compared with the conventional structure.

Thermoplastic polyamide is attached to both sides of polyimide base material, which is first glued to lead frame, and a DRAM chip is die-bonded to the other side by a newly developed LOC mounter. After that, it is processed in the conventional assembly and mold technology.

Comparison of COL/LOC package structures: Large dies can be mounted and multi power sourcing can be provided by LOC structure, thereby realizing higher speed.

項目		Conventional	COL	LOC
Structure	Description			
Lead frame	Die pad	Yes	No	No
	Insulating film	No	Yes	Yes
Wire bond	2nd bond	4 sides of chip	2 sides of chip	All inside the chip area
	長さ(mm)	2.0~3.0	2.0~2.5	0.2~2.0
Die bond	Large die	Stress unbalance betw. leads	Stress relief by ins. film	Stress relief by ins. film
大ペレット，収納化率		△	○	◎
最大素子収納率		60%	70%	90%
高速化		○	○	◎
マルチ電源化		△	△	◎
信頼性		○	○	○
技術的難易度		小	中	大

注：略語説明など COL (Chip On Lead), LOC (Lead On Chip), メリット大◎→○→△小



Example of 4M DRAM adopting LOC structure (X-ray photograph)

In LOC structure, all the wires are bonded within the die area, and it becomes possible to mount large dies in small packages.

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