To search page

1991

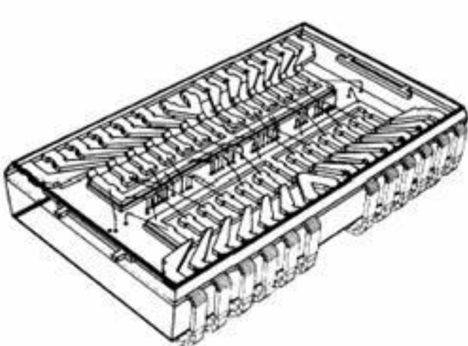
Announcement of the adoption of an LOC structure for 16-Mbyte DRAM

~ Packaging ~

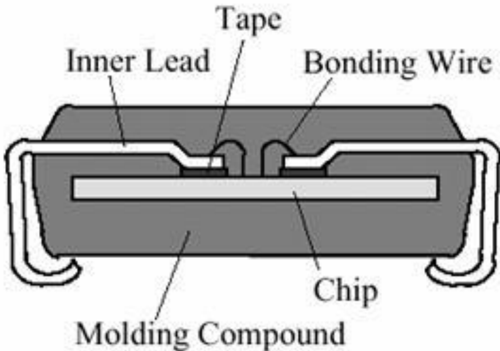
In 1988, Hitachi and TI started the joint project GT (Get Together), as a project after reconciliation of DRAM patent litigation, in which the LOC (Lead On Chip) technology was applied to 16M DRAM . The LOC was a packaging technology developed by Hitachi to mount a large die in a small outline package. Hitachi and TI jointly announced the successful development and its application to 16MDRAM in February 1991 issue of Nikkei Microdevice.

In the LOC structure, the lead frame is die-bonded over the surface of the DRAM chip with an adhesive, and gold wire bonding between the lead frame and the chip is performed within the device area. It provides advantages such as high-speed data transmission, high moisture resistance reliability, reduction in element size etc., and was then adopted as a basic package of 16 MDRAM and subsequent generations. TI adopted it from 4M generation in full scale.

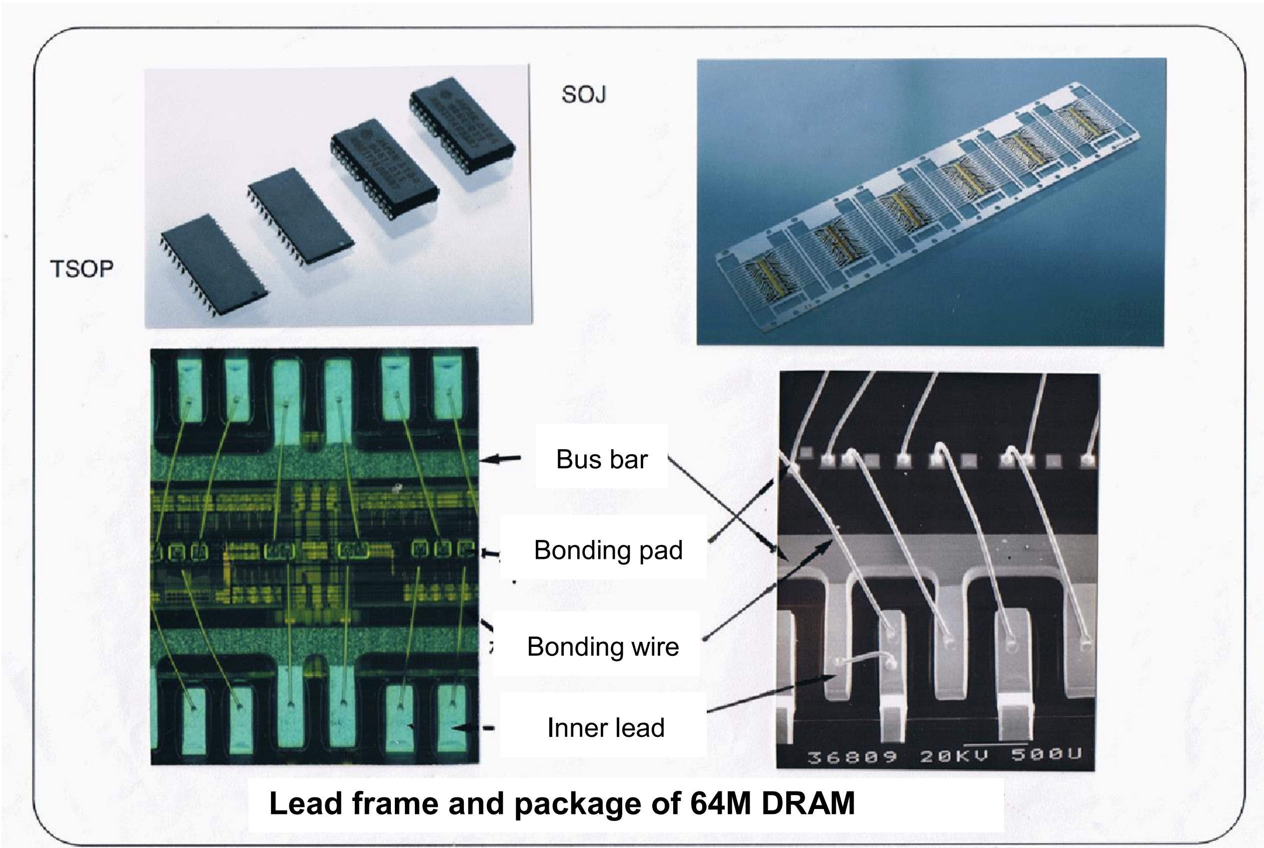
The figures below show a bird's view and a cross section of the LOC structure, and the bottom pictures show the 64 M DRAM application. The LOC structure was developed with the full strength of the Hitachi group, and the related businesses expanded, namely, Hitachi Chemical in the adhesive tapes, Hitachi Cable in the lead frames, and Hitachi Tokyo Electronics in the LOC bonder equipment. LOC technology was transferred to domestic and foreign DRAM companies through these materials and equipment manufacturers.



a) A bird's eye view



b) a cross section



Lead frame and package of 64M DRAM

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