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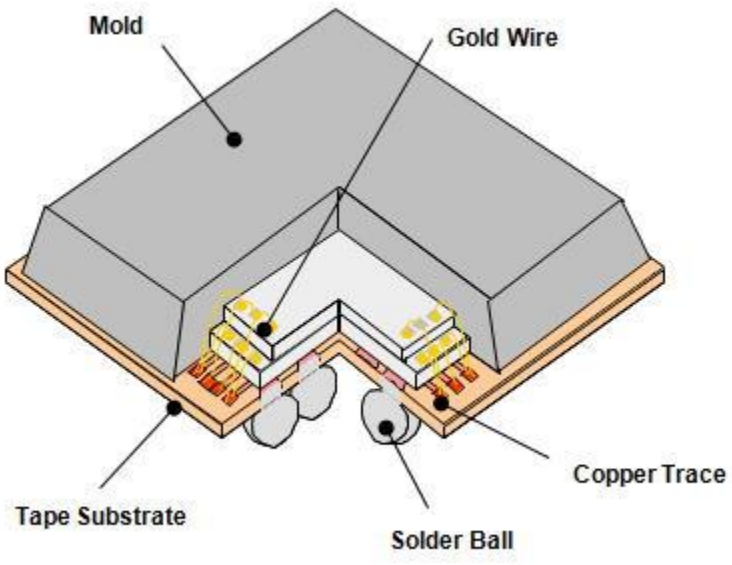
1998
Mass production of stacked CSPs starts
~ Packaging ~

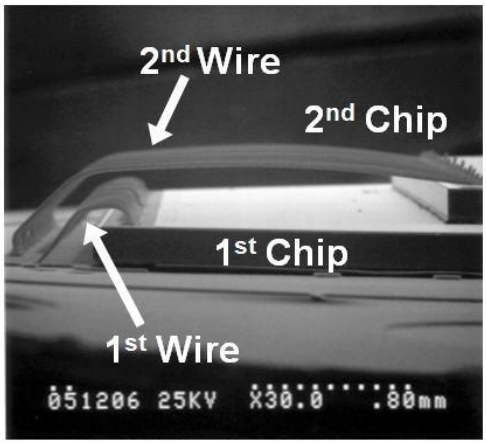
In April 1998, Sharp announced mass-production of stacked CSP stacking two LSI chips. 16 Mbit Flash EEPROM and 2 Mbit SRAM were installed. Package outline was 8 mm ×10 mm, and the weight was 0.17 g, with the reduction by 57% and 80% respectively, compared to tape CSP.

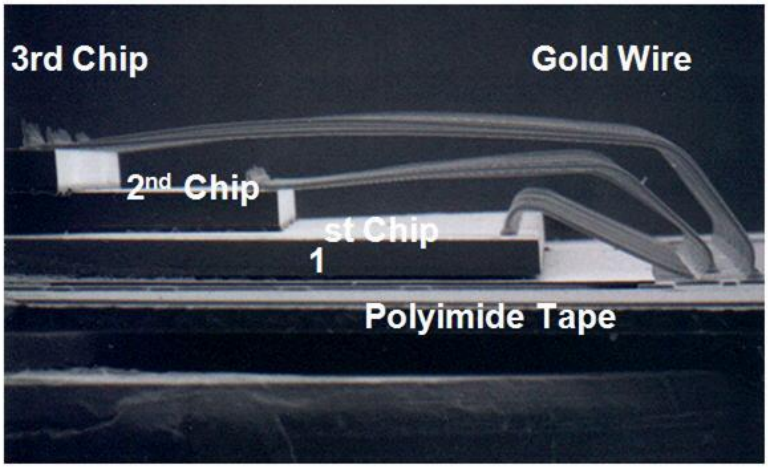
In July 1999, Sharp further announced a plan to mass-produce 3-stack CSP which stacked three components such as control LSI (baseband), Flash memory (32Mbit) and SRAM (8Mbit) from August. The thickness of the LSI chips was reduced to 150 μm, and reverse bonding was applied to the second and third chips to reduce the height of the bonded wires.

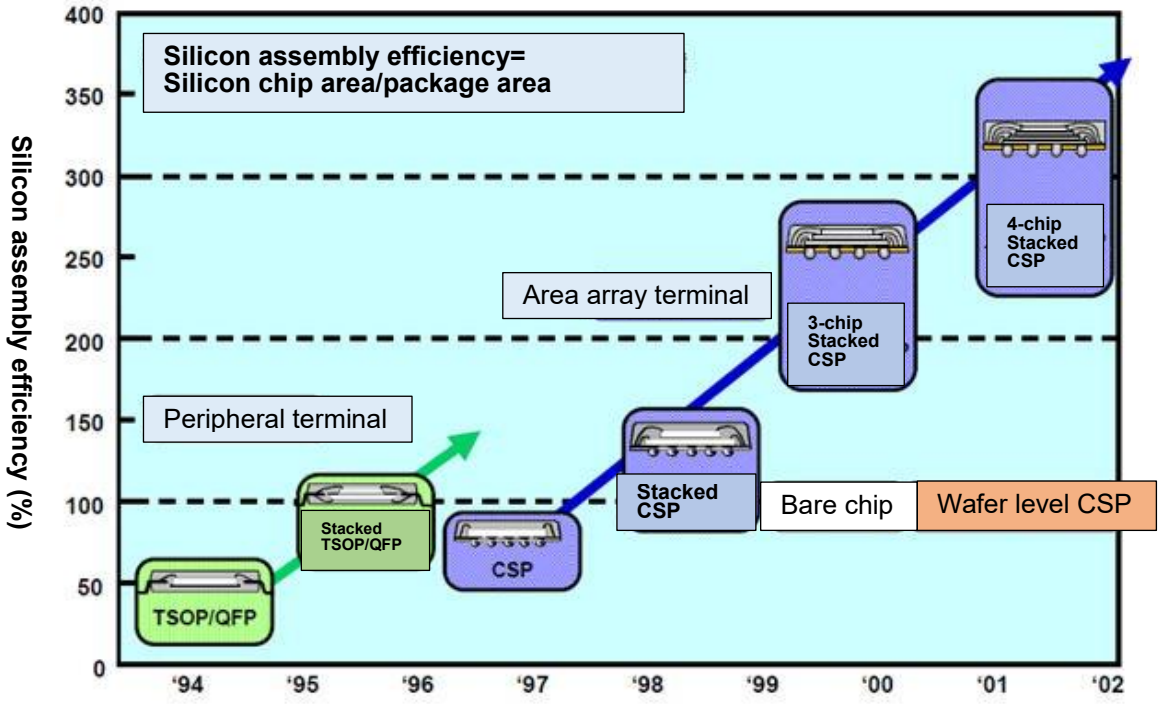
The company led the era of multilayer CSP, by realizing four-chip-stack and so on, and it commercialized various unique mobile devices such as mobile phones by applying this technology.

The figures below show the stacked CSP structure schematic diagram, SEM photograph of 2 element stacked CSP, that of 3 element stack, and the product evolution.




2nd Wire
2nd Chip
1st Chip
1st Wire
051206 25KV X30.0 .80mm


3rd Chip
Gold Wire
2nd Chip
st Chip
1
Polyimide Tape


Silicon assembly efficiency (%)
400
350
300
250
200
150
100
50
0
Silicon assembly efficiency=
Silicon chip area/package area
Area array terminal
Peripheral terminal
TSOP/QFP
Stacked TSOP/QFP
CSP
Stacked CSP
3-chip Stacked CSP
4-chip Stacked CSP
Bare chip
Wafer level CSP
'94
'95
'96
'97
'98
'99
'00
'01
'02