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Late 1960s

Application of CVD oxide films for low noise device process

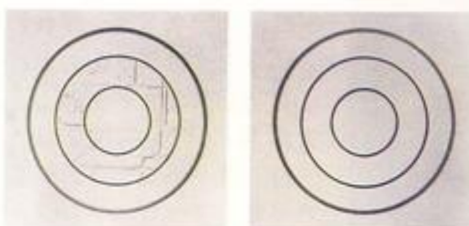
~ Process Technology ~

Conventionally, silicon was oxidized at high temperature to form a silicon dioxide film on the surface, but deposition of a silicon oxide film became possible by the CVD method, and new application were developed. Among such applications, the technology to reduce noise in transistors and ICs became one of the drivers of Japanese semiconductor industry, contributing significantly to the development of consumer electronics.

In 1966, Hitachi developed LTP (Low Temperature Passivation) technology in which a thermal oxide film was removed and a CVD oxide film was formed on the removed surface instead, which was then given thermal treatment. If the CVD oxide film is directly attached to silicon, its interface becomes mismatched with silicon (technically speaking, the surface states increase) to cause electrical noise, but in the LTP technology, heat treatment conditions were optimized to greatly reduce the surface states. By this technology, low noise transistors and low noise ICs were developed, and contributed greatly to the development of solid-state audio equipment and the like in Japan.

From around 1968, Toshiba worked on the development of technology of defect-free diffusion using CVD oxide films in order to reduce crystal defects, which were one of the causes of noise. In the development of technology to deposit doped CVD oxide film (oxide film containing diffusion impurity) directly on the silicon surface and to perform diffusion using this film as a diffusion source, they found that addition of Arsenic in optimized concentration to phosphorus would reduce defect density, and they developed the PCT technology (Perfect Crystal Technology as they called it) in 1970. Low noise transistors and low noise ICs were commercialized by PCT technology. Since CVD films were directly deposited on the Si surface like in LTP technology, and the optimize heat treatments were important know-hows, it is estimated that reduction of the interface states also contributed to low noise characteristics in PCT

Both LTP and PCT were valued also as technologies to avoid the use of Fairchild's planar patent.



(a) (b)

(a) Transistor by conventional process
(Vertical and horizontal lines are seen)
(b) Transistor by PCT process
(No crystal defect is observed)

Figure: Reduction of crystal defects by PCT process

Reference:

1) M. Watanabe, T. Yonezawa, M. Nakamura, T. Kato and M. Akatsuka:
Inst. Electron, Common. Engrs. Japan SSD-7-13 (1970)

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