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Late 1980s

Applying three-dimensional cell structures to DRAM

~ Process Technology ~

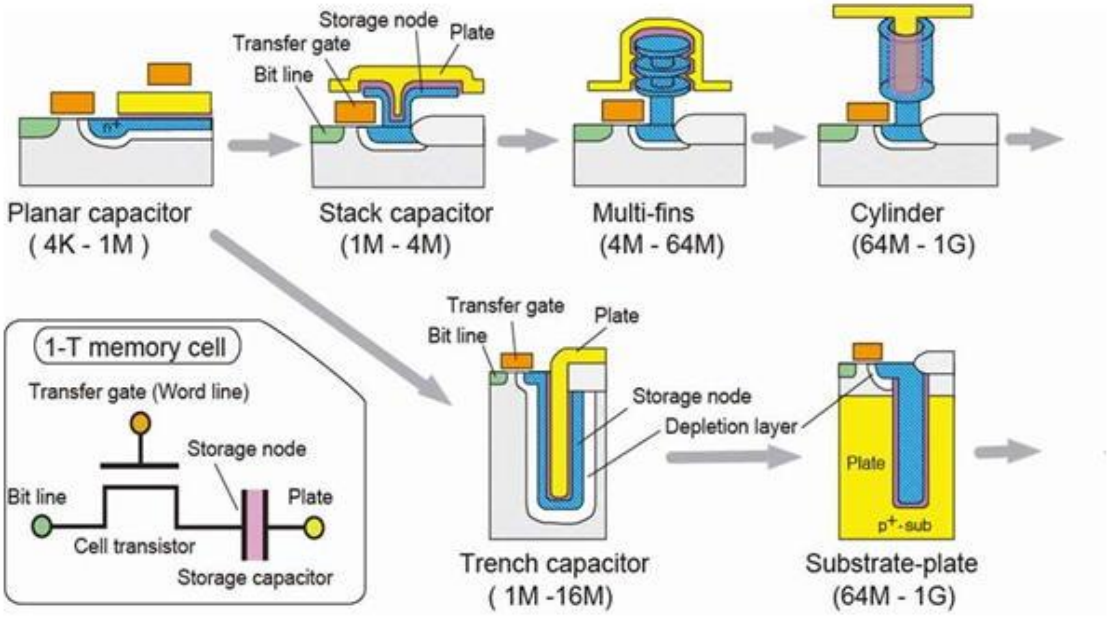
DRAM (Dynamic Random Access Memory) is a memory device that stores information by storing electric charges in the capacitors, and since 1K bit DRAM was commercialized by Intel in 1970, the memory densities have been quadrupled in every 3 years as one generation. Each time the generation progressed, the chip area has been expanded to 1.4 times, memory cells have been reduced to almost 1/3, and the degree of integration has been doubled. In order to reduce the area of the memory cell, the area of the charge storage capacitor must also be reduced. On the other hand, since the memory cell capacitance value must be maintained for a stable memory operation, the thickness of the capacitor insulating film has been reduced to compensate the size reduction. In order to make the insulating film thinner, a method of lowering the voltage applied to the insulating film has been adopted ("half Vcc" plate voltage method).

In the megabit generations in the latter half of the 1980s, finally, planar cells that formed planar MOS capacitors on the surface of Si substrates could no longer secure the required capacitance value, so that three-dimensional cells were adopted. There are trench cells and stack cells as the three-dimensional cell structures, both of which were invented in Japan in the 1970s.
The trench cell has the cell structure that secures the capacitance value by forming a groove perpendicular to the Si substrate and forming a capacitor on the side wall. It was invented by Hideo Sunami of Hitachi in 1975 and the prototype result was presented at the International Electronic Devices Meeting (IEDM) in 1982. In the late 1980s, Toshiba, IBM, Siemens, TI etc., commercialized 1 Mbit DRAM by applying this technology.

The stacked cell is a cell structure securing the capacitance value by three-dimensionally stacked capacitors on the switching transistors, which was invented by Mitsumasa Koyanagi of Hitachi in 1976, and the prototype result was presented at IEDM in 1978. Fujitsu led in the commercialization in 1 Mbit applying this technology in 1985, followed by Hitachi, Mitsubishi, Samsung, Gold Star, Hyundai, Micron and NEC in 4 Mbit. From the 2000 onwards, most of DRAMs were made by applying the stack cells that are advantageous for miniaturization.

As a technique for miniaturizing stacked cells, HSG Poly-Si (Hemi-spherical grained Poly-Si) technology, which increases the effective surface area per unit two-dimensional area by forming irregularities on the surface of polycrystalline Si was also invented in Japan. NEC reported the concept at the International Solid State Device and Materials Conference (SSDM) in 1990, announced it as one

of the 256 Mbit technologies at IEDM in 1992, and succeeded in mass production in 64 Mbit in 1996. By 2001, 70% of DRAM manufacturers adopted HSG Poly-Si. As shown above, most of the basic technologies of the megabit generation DRAM memory cell were invented in Japan, and in the latter half of the 1980s, 80% of world DRAM production share, and more than 50% of total semiconductors were occupied by Japanese manufacturers.



Formation of three-dimensional DRAM cell structures

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