To search page

Middle of 1980s

Transition of flattening technique from reflow to etching back

~ Process Technology ~

In the reflow method used since the 1970s, the processing temperature was high (about 800°C even using BPSG), and it became incompatible with the lowering of the process temperatures accompanying the progress of miniaturization. In particular, multilayer interconnect of Al came to be increasingly used as the degree of integration was increased, but a high temperature reflow process could not be used for flattening the insulating film between the interconnect layers.

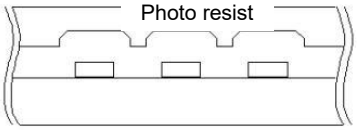
It was the flattening technique by the etch back method that appeared at this time. In the etch-back method, a photoresist is spin-coated (a liquid photoresist is dropped onto a wafer rotating at high speed and covering the wafer) on a CVD insulating film having convexo-concave forms, and the wafer is etched over the entire surface with a plasma etching apparatus. The spin-coated photoresist fills the unevenness of the substrate and the surface is flattened, which then is scraped off by plasma etching (this process is called an etch-back process because it removes the photoresist once attached). At this time, the etching is performed under the condition that the etching rate of the photoresist and the underlying CVD insulating film are the same, and the CVD insulating film is scraped off and flattened with the original flat surface of the photoresist. Note that SOG (spin-on-glass, coating type insulating film) was often used together in the etch-back process, in order to alleviate irregularities of the underlying CVD insulating film in advance.

The reason why the etch-back method was put into practical use is that an anisotropic plasma etching apparatus came to be widely used in the mid-1980s, and isotropic plasma etching could also be used for planarization. By using an anisotropic plasma etching equipment (RIE), application of etch-back technology for other purposes different from planarization was developed.

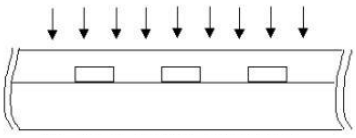
Specifically, a CVD insulating film is formed after formation of the polysilicon gate, and the etch-back is performed by RIE (without applying photoresist, unlike planarization), thereby only the sidewall of the gate is left unremoved. This technique became an important technology in miniaturization at later time.

In the latter half of the 1990s, further planarization was required, and the planarization by CMP was started.

(1) Deposition of CVD insulating film



(2) Spin-coat of photoresist



(3) Flattening by plasma etching

Version 2019/1/13